

# DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

## **HEF4014B**

## **MSI**

## **8-bit static shift register**

Product specification  
File under Integrated Circuits, IC04

January 1995

8-bit static shift register

HEF4014B  
MSI

DESCRIPTION

The HEF4014B is a fully synchronous edge-triggered 8-bit static shift register with eight synchronous parallel inputs (P<sub>0</sub> to P<sub>7</sub>), a synchronous serial data input (D<sub>S</sub>), a synchronous parallel enable input (PE), a LOW to HIGH edge-triggered clock input (CP) and buffered parallel outputs from the last three stages (O<sub>5</sub> to O<sub>7</sub>).

Operation is synchronous and the device is edge-triggered on the LOW to HIGH transition of CP. Each register stage is of a D-type master-slave flip-flop. When PE is HIGH, data is loaded into the register from P<sub>0</sub> to P<sub>7</sub> on the LOW to HIGH transition of CP. When PE is LOW, data is shifted to the first position from D<sub>S</sub>, and all the data in the register is shifted one position to the right on the LOW to HIGH transition of CP. Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times

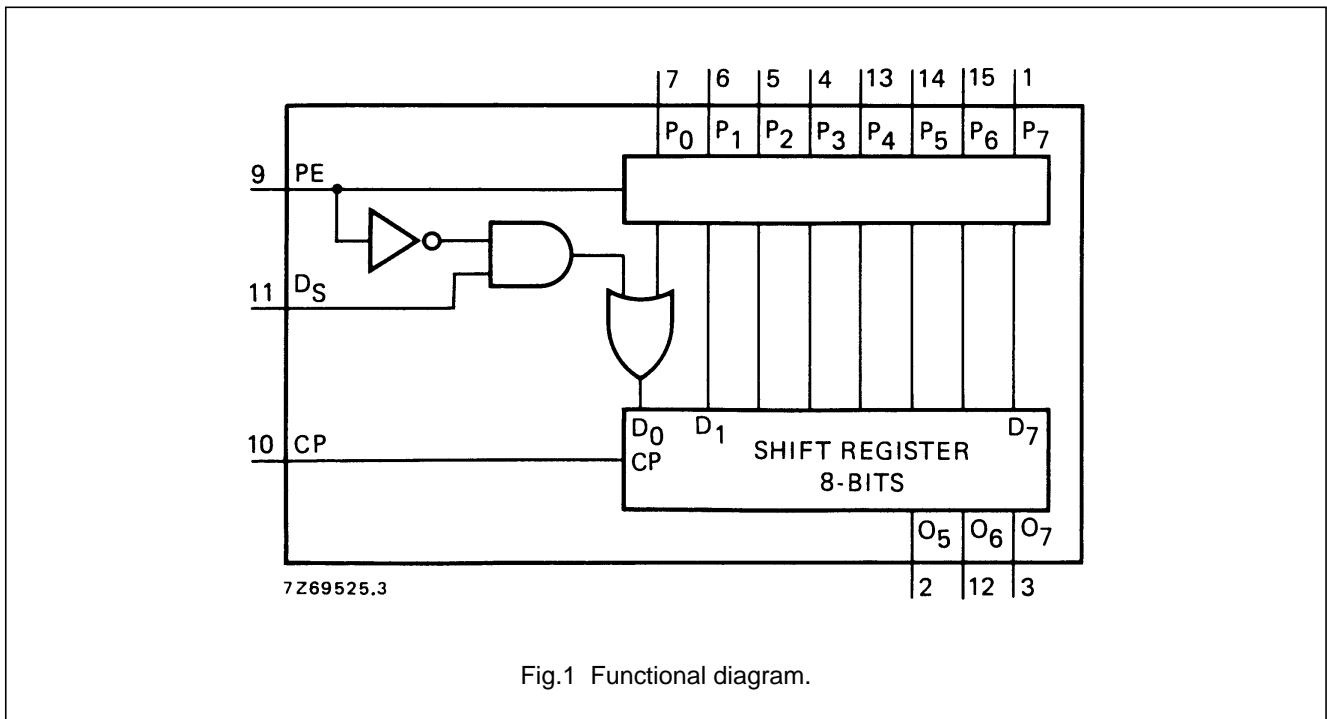


Fig.1 Functional diagram.

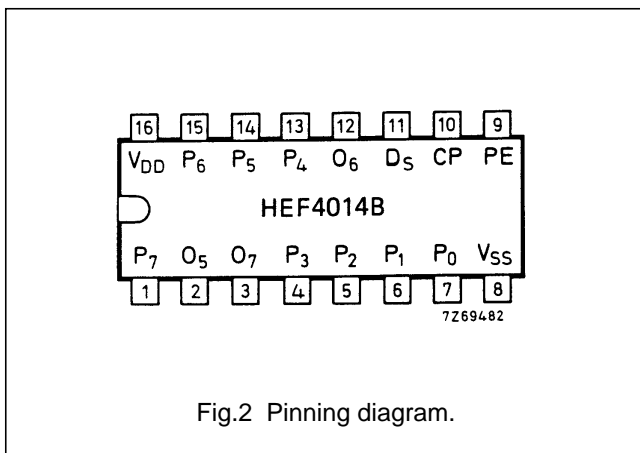


Fig.2 Pinning diagram.

- HEF4014BP(N): 16-lead DIL; plastic (SOT38-1)
- HEF4014BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
- HEF4014BT(D): 16-lead SO; plastic (SOT109-1)
- ( ): Package Designator North America

FAMILY DATA, I<sub>DD</sub> LIMITS category MSI

See Family Specifications



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## PINNING

- PE parallel enable input
- P<sub>0</sub> to P<sub>7</sub> parallel data inputs
- D<sub>S</sub> serial data input
- CP clock input (LOW to HIGH edge-triggered)
- O<sub>5</sub> to O<sub>7</sub> buffered parallel outputs from the last three stages

## FUNCTION TABLES

Serial operation

n	INPUTS			OUTPUTS		
	CP	D <sub>S</sub>	PE	O <sub>5</sub>	O <sub>6</sub>	O <sub>7</sub>
1		D <sub>1</sub>	L	X	X	X
2		D <sub>2</sub>	L	X	X	X
3		D <sub>3</sub>	L	X	X	X
6		X	L	D <sub>1</sub>	X	X
7		X	L	D <sub>2</sub>	D <sub>1</sub>	X
8		X	L	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>
		X	X	no change		

Parallel operation

n	INPUTS			OUTPUTS		
	CP	D <sub>S</sub>	PE	O <sub>5</sub>	O <sub>6</sub>	O <sub>7</sub>
1		X	H	P <sub>5</sub>	P <sub>6</sub>	P <sub>7</sub>
		X	X	no change		

### Notes

1. H = HIGH state (the more positive voltage)  
 L = LOW state (the less positive voltage)  
 X = state is immaterial
- = positive-going transition  
 = negative-going transition  
 D<sub>n</sub> = either HIGH or LOW  
 n = number of clock pulse transitions

## AC CHARACTERISTICS

V<sub>SS</sub> = 0 V; T<sub>amb</sub> = 25 °C; C<sub>L</sub> = 50 pF; input transition times ≤ 20 ns

	V <sub>DD</sub> V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5 10 15	900 f <sub>i</sub> + ∑ (f <sub>o</sub> C <sub>L</sub> ) × V <sub>DD</sub> <sup>2</sup> 4 300 f <sub>i</sub> + ∑ (f <sub>o</sub> C <sub>L</sub> ) × V <sub>DD</sub> <sup>2</sup> 12 000 f <sub>i</sub> + ∑ (f <sub>o</sub> C <sub>L</sub> ) × V <sub>DD</sub> <sup>2</sup>	where f <sub>i</sub> = input freq. (MHz) f <sub>o</sub> = output freq. (MHz) C <sub>L</sub> = load cap. (pF) ∑ (f <sub>o</sub> C <sub>L</sub> ) = sum of outputs V <sub>DD</sub> = supply voltage (V)

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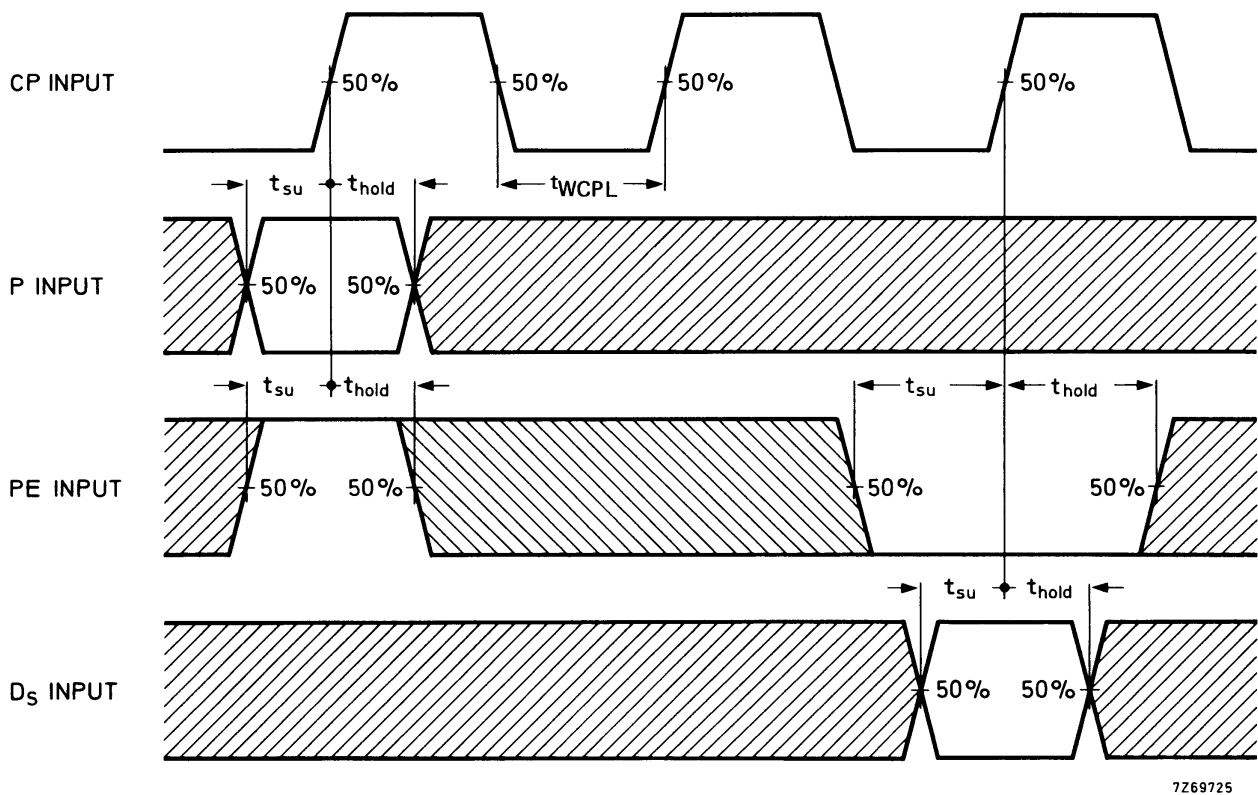
## AC CHARACTERISTICS

 $V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $C_L = 50\text{ pF}$ ; input transition times  $\leq 20\text{ ns}$ 

	$V_{DD}$ V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA	
Propagation delays $C_P \rightarrow O_n$ HIGH to LOW	5	$t_{PHL}$		130	260	ns	$103\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10			55	110	ns	$44\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			40	80	ns	$32\text{ ns} + (0,16\text{ ns/pF}) C_L$
LOW to HIGH	5	$t_{PLH}$		115	230	ns	$88\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10			50	100	ns	$39\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			40	80	ns	$32\text{ ns} + (0,16\text{ ns/pF}) C_L$
Output transition times HIGH to LOW	5	$t_{THL}$		60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10			30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$
	15			20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$
LOW to HIGH	5	$t_{TLH}$		60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10			30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$
	15			20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$
Set-up times PE $\rightarrow$ CP	5	$t_{su}$	40	10		ns	see also waveforms Fig.4
	10		25	5		ns	
	15		15	0		ns	
$D_S \rightarrow CP$	5	$t_{su}$	35	-5		ns	
	10		25	-5		ns	
	15		25	0		ns	
$P_n \rightarrow CP$	5	$t_{su}$	35	-5		ns	
	10		25	-5		ns	
	15		25	0		ns	
Hold times PE $\rightarrow$ CP	5	$t_{hold}$	25	-5		ns	
	10		20	0		ns	
	15		15	0		ns	
$D_S \rightarrow CP$	5	$t_{hold}$	30	15		ns	
	10		20	10		ns	
	15		15	7		ns	
$P_n \rightarrow CP$	5	$t_{hold}$	30	15		ns	
	10		20	10		ns	
	15		15	7		ns	
Minimum clock pulse width; LOW	5	$t_{WCPL}$	70	35		ns	
	10		30	15		ns	
	15		24	12		ns	
Maximum clock pulse frequency	5	$f_{max}$	6	13		MHz	
	10		15	30		MHz	
	15		20	40		MHz	

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Fig.4 Waveforms showing minimum clock pulse width, and set-up and hold times for PE to CP, D<sub>S</sub> to CP, and P to CP. Set-up and hold times are shown as positive values but may be specified as negative values.

**APPLICATION INFORMATION**

Some examples of applications for the HEF4014B are:

- Parallel-to-serial converter
- Serial data queueing
- General purpose register