

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4008B **MSI** 4-bit binary full adder

Product specification
File under Integrated Circuits, IC04

January 1995

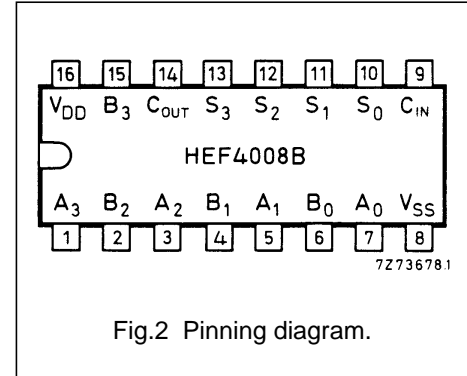
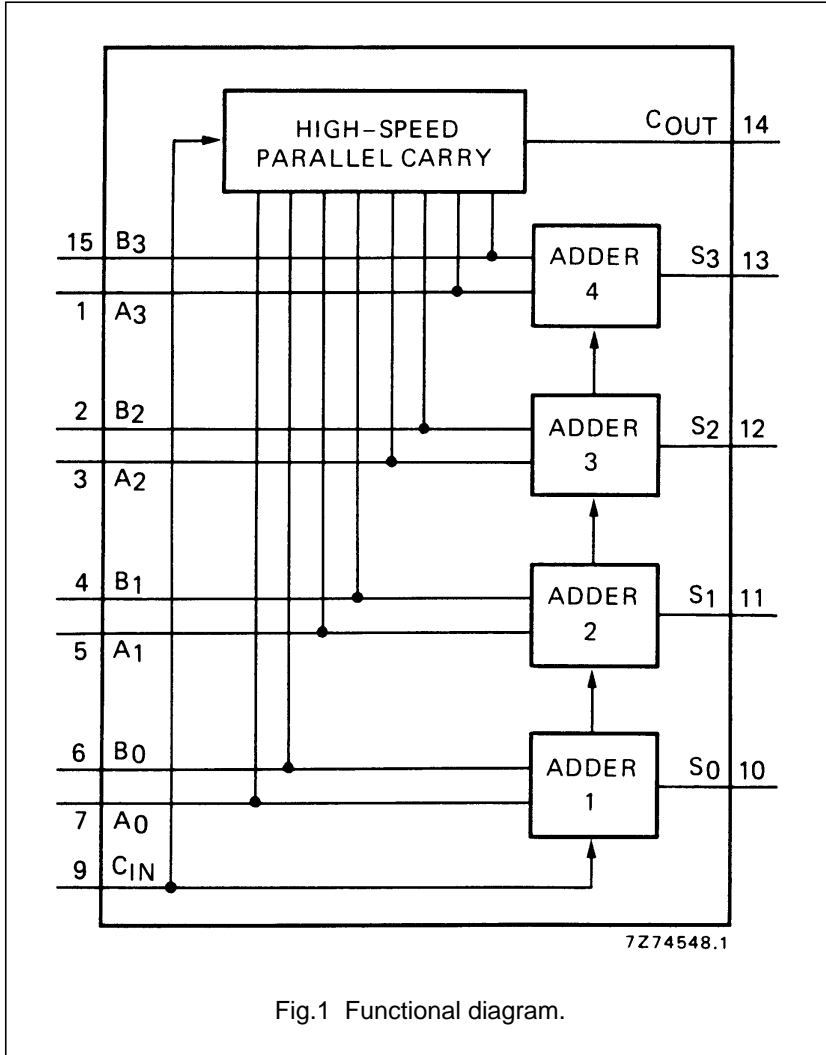
4-bit binary full adder

HEF4008B MSI

DESCRIPTION

The HEF4008B is a 4-bit binary full adder with two 4-bit data inputs (A_0 to A_3 , B_0 to B_3), a carry input (C_{IN}), four sum outputs (S_0 to S_3), and a carry

output (C_{OUT}). The IC uses full look-ahead across 4-bits to generate C_{OUT} . This minimizes the necessity for extensive look-ahead and carry-cascading circuits.



PINNING

- A_0 to A_3 data inputs
- B_0 to B_3 data inputs
- S_0 to S_3 sum outputs
- C_{IN} carry input
- C_{OUT} carry output

TRUTH TABLE (one adder)

| C_{IN} | A | B | C_{OUT} | S |
|----------|---|---|-----------|---|
| L | L | L | L | L |
| L | L | H | L | H |
| L | H | L | L | H |
| L | H | H | H | L |
| H | L | L | L | H |
| H | L | H | H | L |
| H | H | L | H | L |
| H | H | H | H | H |

- HEF4008BP(N): 16-lead DIL; plastic (SOT38-1)
- HEF4008BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
- HEF4008BT(D): 16-lead SO; plastic (SOT109-1)
- (): Package Designator North America

FAMILY DATA, I_{DD} LIMITS category MSI

See Family Specifications

4-bit binary full adder

HEF4008B
MSI

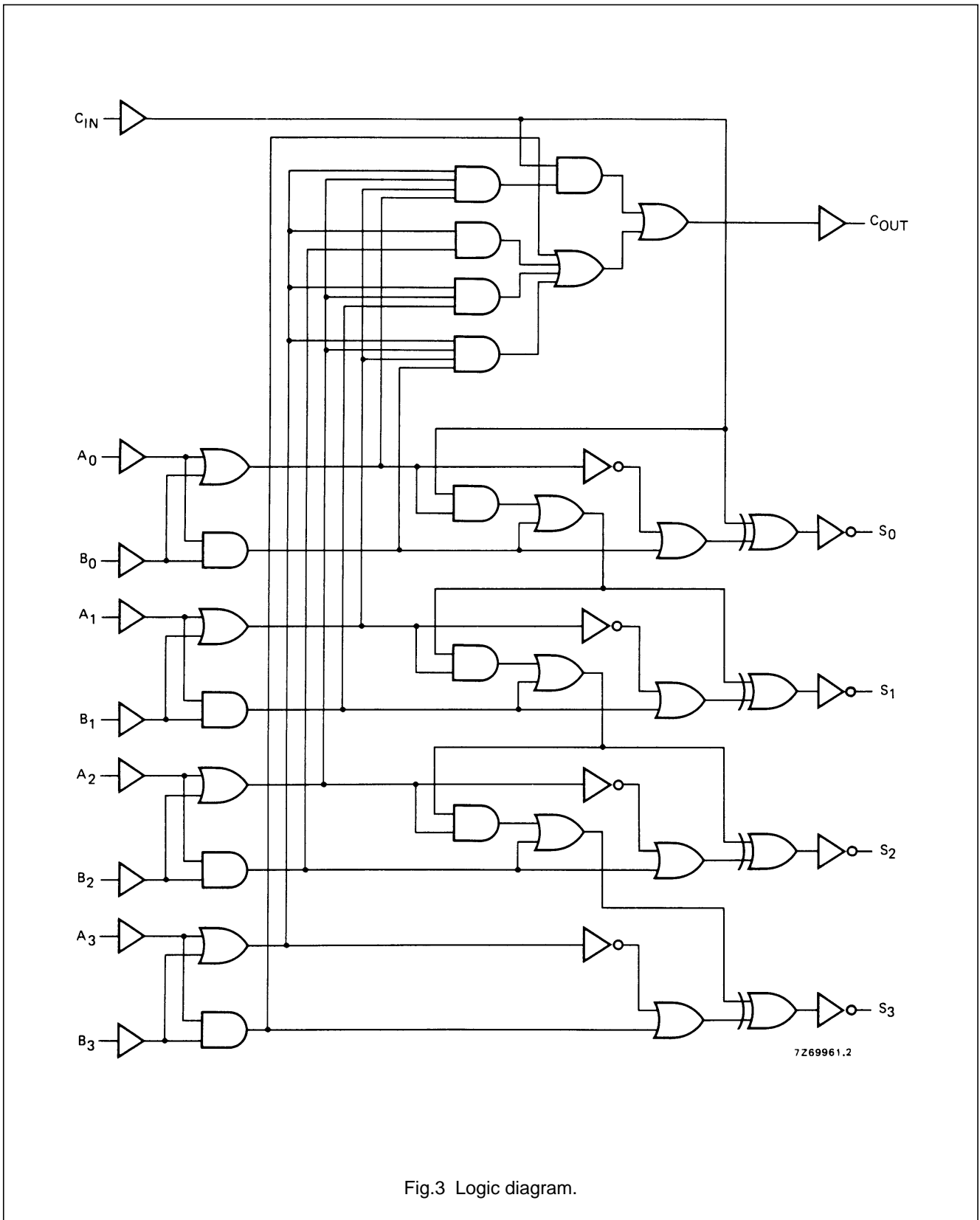


Fig.3 Logic diagram.

4-bit binary full adder

HEF4008B
MSI**AC CHARACTERISTICS** $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ °C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

| | V_{DD} V | SYMBOL | MIN. | TYP. | MAX. | TYPICAL EXTRAPOLATION FORMULA | |
|---|---------------|-----------|------|------|------|----------------------------------|-----------------------------|
| Propagation delays sum in \rightarrow sum out HIGH to LOW | 5 | t_{PHL} | | 150 | 300 | ns | 123 ns + (0,55 ns/pF) C_L |
| | 10 | | | 55 | 110 | ns | 44 ns + (0,23 ns/pF) C_L |
| | 15 | | | 40 | 80 | ns | 32 ns + (0,16 ns/pF) C_L |
| LOW to HIGH | 5 | t_{PLH} | | 135 | 270 | ns | 108 ns + (0,55 ns/pF) C_L |
| | 10 | | | 55 | 110 | ns | 44 ns + (0,23 ns/pF) C_L |
| | 15 | | | 40 | 80 | ns | 32 ns + (0,16 ns/pF) C_L |
| sum in \rightarrow C_{OUT} HIGH to LOW | 5 | t_{PHL} | | 125 | 250 | ns | 98 ns + (0,55 ns/pF) C_L |
| | 10 | | | 50 | 100 | ns | 39 ns + (0,23 ns/pF) C_L |
| | 15 | | | 35 | 70 | ns | 27 ns + (0,16 ns/pF) C_L |
| LOW to HIGH | 5 | t_{PLH} | | 100 | 200 | ns | 73 ns + (0,55 ns/pF) C_L |
| | 10 | | | 45 | 90 | ns | 34 ns + (0,23 ns/pF) C_L |
| | 15 | | | 30 | 60 | ns | 22 ns + (0,16 ns/pF) C_L |
| $C_{IN} \rightarrow$ sum out HIGH to LOW | 5 | t_{PHL} | | 130 | 260 | ns | 103 ns + (0,55 ns/pF) C_L |
| | 10 | | | 50 | 100 | ns | 39 ns + (0,23 ns/pF) C_L |
| | 15 | | | 35 | 70 | ns | 27 ns + (0,16 ns/pF) C_L |
| LOW to HIGH | 5 | t_{PLH} | | 115 | 230 | ns | 88 ns + (0,55 ns/pF) C_L |
| | 10 | | | 50 | 100 | ns | 39 ns + (0,23 ns/pF) C_L |
| | 15 | | | 35 | 70 | ns | 27 ns + (0,16 ns/pF) C_L |
| $C_{IN} \rightarrow C_{OUT}$ HIGH to LOW | 5 | t_{PHL} | | 90 | 180 | ns | 63 ns + (0,55 ns/pF) C_L |
| | 10 | | | 35 | 70 | ns | 24 ns + (0,23 ns/pF) C_L |
| | 15 | | | 25 | 50 | ns | 17 ns + (0,16 ns/pF) C_L |
| LOW to HIGH | 5 | t_{PLH} | | 75 | 150 | ns | 48 ns + (0,55 ns/pF) C_L |
| | 10 | | | 35 | 70 | ns | 24 ns + (0,23 ns/pF) C_L |
| | 15 | | | 25 | 50 | ns | 17 ns + (0,16 ns/pF) C_L |
| Output transition times HIGH to LOW | 5 | t_{THL} | | 60 | 120 | ns | 10 ns + (1,0 ns/pF) C_L |
| | 10 | | | 30 | 60 | ns | 9 ns + (0,42 ns/pF) C_L |
| | 15 | | | 20 | 40 | ns | 6 ns + (0,28 ns/pF) C_L |
| LOW to HIGH | 5 | t_{TLH} | | 60 | 120 | ns | 10 ns + (1,0 ns/pF) C_L |
| | 10 | | | 30 | 60 | ns | 9 ns + (0,42 ns/pF) C_L |
| | 15 | | | 20 | 40 | ns | 6 ns + (0,28 ns/pF) C_L |

4-bit binary full adder

HEF4008B
MSI

| | V _{DD} V | TYPICAL FORMULA FOR P (μW) | |
|---|----------------------|---|---|
| Dynamic power dissipation per package (P) | 5 10 15 | 1 500 f _i + ∑ (f _o C _L) × V _{DD} ² 6 000 f _i + ∑ (f _o C _L) × V _{DD} ² 13 500 f _i + ∑ (f _o C _L) × V _{DD} ² | where f _i = input freq. (MHz) f _o = output freq. (MHz) C _L = load capacitance (pF) ∑ (f _o C _L) = sum of outputs V _{DD} = supply voltage (V) |

APPLICATION INFORMATION

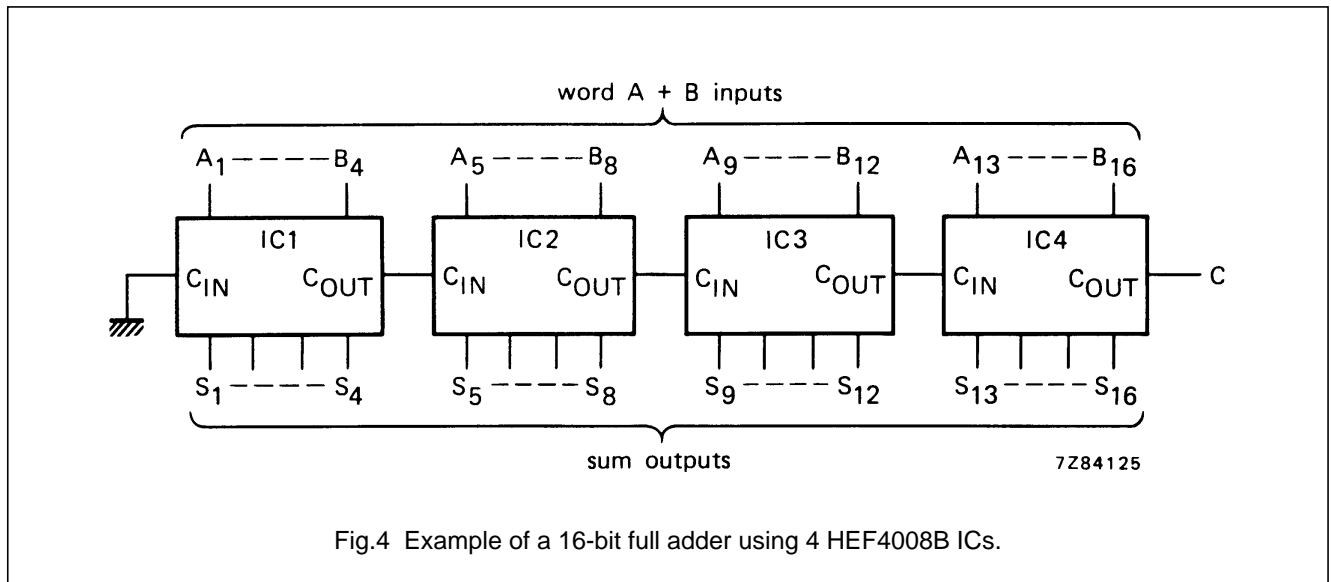


Fig.4 Example of a 16-bit full adder using 4 HEF4008B ICs.