

# DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

## HEF4043B

### MSI

## Quadruple R/S latch with 3-state outputs

Product specification  
File under Integrated Circuits, IC04

January 1995

# Quadruple R/S latch with 3-state outputs

## HEF4043B MSI

### DESCRIPTION

The HEF4043B is a quadruple R/S latch with 3-state outputs with a common output enable input (EO). Each latch has an active HIGH set input (S<sub>0</sub> to S<sub>3</sub>), an active HIGH reset input (R<sub>0</sub> to R<sub>3</sub>) and an active HIGH 3-state output (O<sub>0</sub> to O<sub>3</sub>).

When EO is HIGH, the state of the latch output (O<sub>n</sub>) can be determined from the function table below. When EO is LOW, the latch outputs are in the high impedance OFF-state. EO does not affect the state of the latch.

The high impedance off-state feature allows common bussing of the outputs.

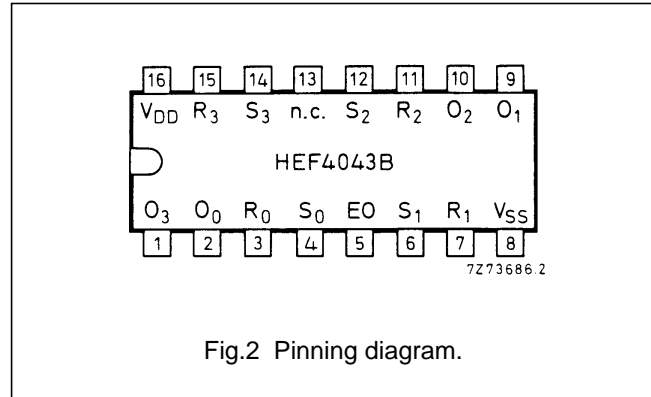


Fig.2 Pinning diagram.

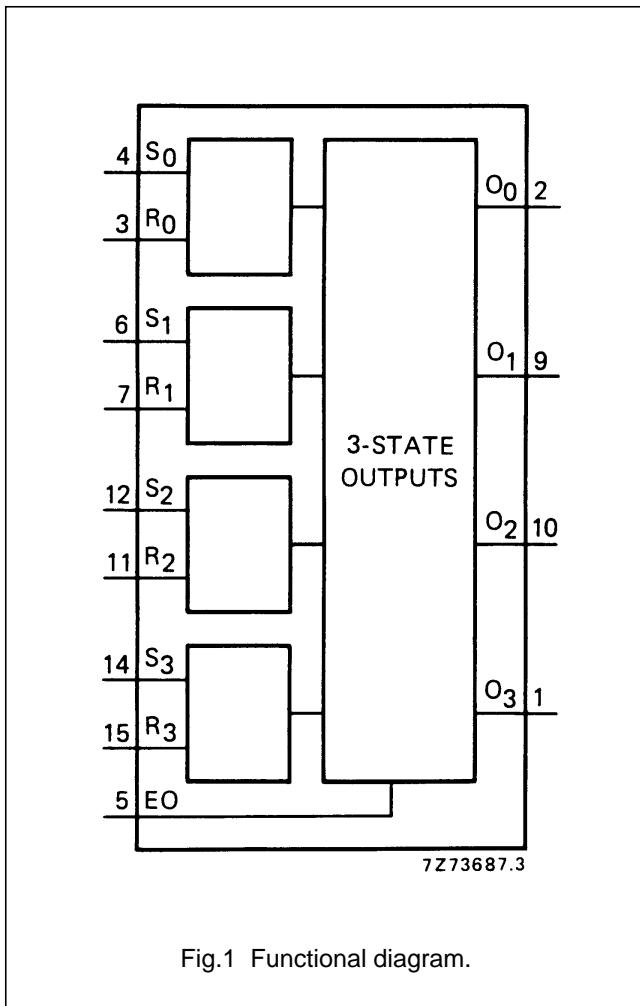


Fig.1 Functional diagram.

- HEF4043BP(N): 16-lead DIL; plastic (SOT38-1)
- HEF4043BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
- HEF4043BT(D): 16-lead SO; plastic (SOT109-1)
- ( ): Package Designator North America

### PINNING

- EO common output enable input
- S<sub>0</sub> to S<sub>3</sub> set inputs (active HIGH)
- R<sub>0</sub> to R<sub>3</sub> reset inputs (active HIGH)
- O<sub>0</sub> to O<sub>3</sub> 3-state buffered latch outputs

### FUNCTION TABLE

INPUTS			OUTPUT O <sub>n</sub>
EO	S <sub>n</sub>	R <sub>n</sub>	
L	X	X	Z
H	L	H	L
H	H	X	H
H	L	L	latched

### Notes

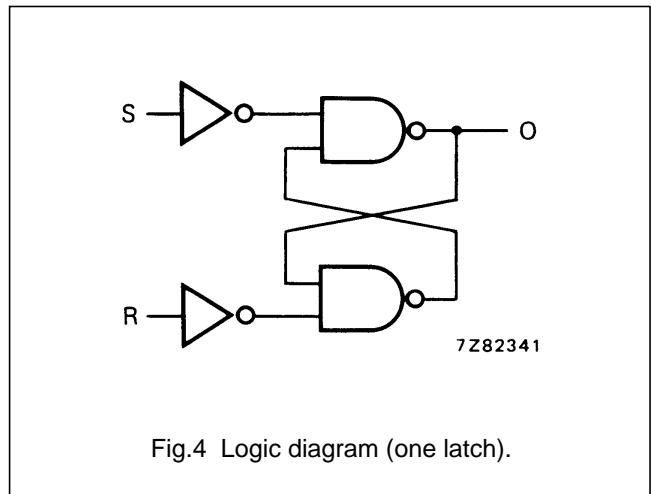
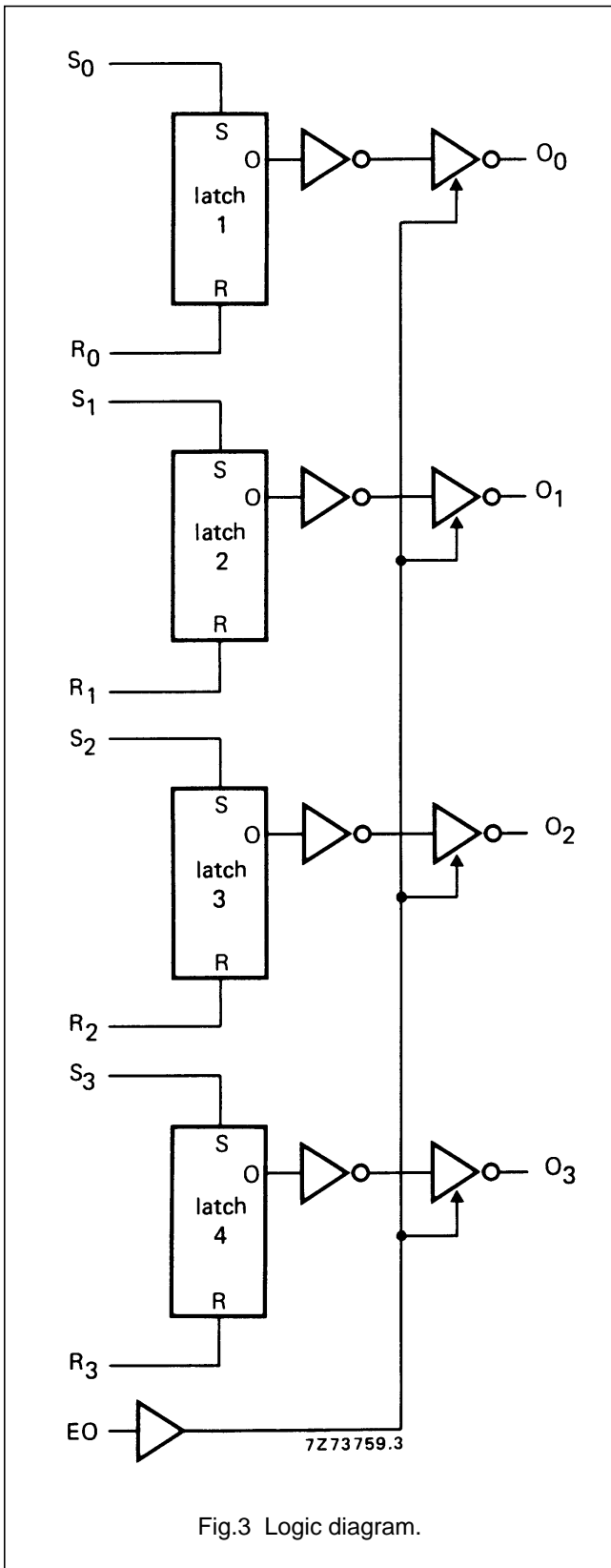
1. H = HIGH state (the more positive voltage)  
 L = LOW state (the less positive voltage)  
 X = state immaterial  
 Z = high impedance state

### FAMILY DATA, I<sub>DD</sub> LIMITS category MSI

See Family Specifications

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### AC CHARACTERISTICS

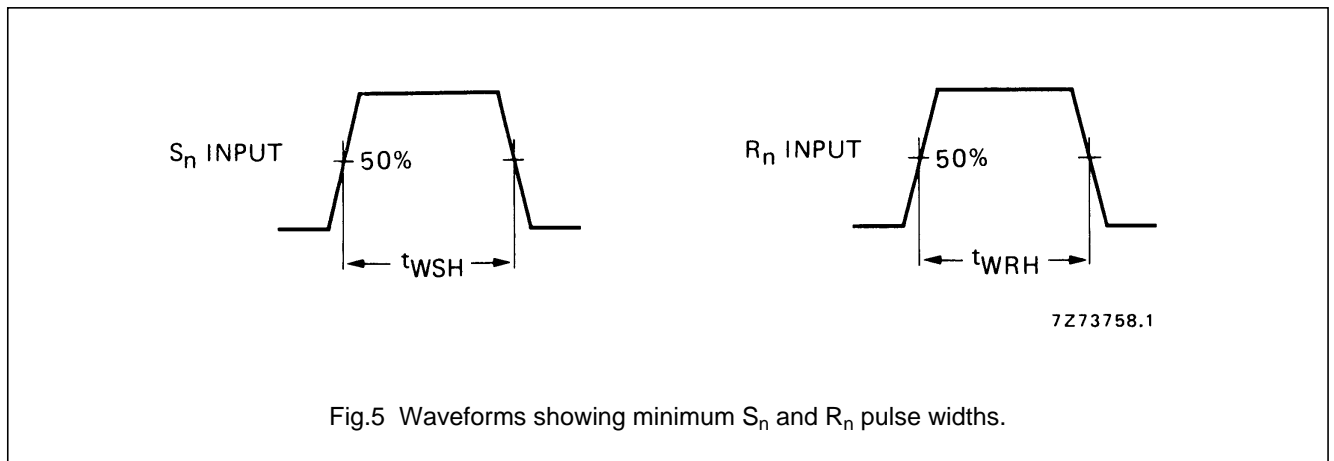
$V_{SS} = 0$  V;  $T_{amb} = 25$  °C;  $C_L = 50$  pF; input transition times  $\leq 20$  ns

	$V_{DD}$ V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA		
Propagation delays $R_n \rightarrow O_n$ HIGH to LOW	5	$t_{PHL}$		90	180	ns	63 ns + (0,55 ns/pF) $C_L$	
	10			35	70	ns		24 ns + (0,23 ns/pF) $C_L$
	15			25	50	ns		17 ns + (0,16 ns/pF) $C_L$
	$S_n \rightarrow O_n$ LOW to HIGH	5	$t_{PLH}$		65	135	ns	38 ns + (0,55 ns/pF) $C_L$
		10			25	50	ns	14 ns + (0,23 ns/pF) $C_L$
		15			15	35	ns	7 ns + (0,16 ns/pF) $C_L$
Output transition times HIGH to LOW	5	$t_{THL}$		60	120	ns	10 ns + (1,0 ns/pF) $C_L$	
	10			30	60	ns	9 ns + (0,42 ns/pF) $C_L$	
	15			20	40	ns	6 ns + (0,28 ns/pF) $C_L$	
	LOW to HIGH	5	$t_{TLH}$		60	120	ns	10 ns + (1,0 ns/pF) $C_L$
		10			30	60	ns	9 ns + (0,42 ns/pF) $C_L$
		15			20	40	ns	6 ns + (0,28 ns/pF) $C_L$
3-state propagation delays Output disable times $EO \rightarrow O_n$ HIGH	5	$t_{PHZ}$		45	90	ns	see also waveforms Fig.5	
	10			20	35	ns		
	15			10	25	ns		
	LOW	5	$t_{PLZ}$		50	100		ns
		10			20	40		ns
		15			10	25		ns
Output enable times $EO \rightarrow O_n$ HIGH	5	$t_{PZH}$		25	50	ns		
	10			15	30	ns		
	15			10	25	ns		
	LOW	5	$t_{PZL}$		40	80	ns	
		10			20	45	ns	
		15			15	35	ns	
Minimum $S_n$ pulse width; HIGH	5	$t_{WSH}$		30	15	ns		
	10			20	10	ns		
	15			16	8	ns		
Minimum $R_n$ pulse width; HIGH	5	$t_{WRH}$		30	15	ns		
	10			20	10	ns		
	15			16	8	ns		

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	$V_{DD}$ V	TYPICAL FORMULA FOR P ( $\mu$ W)	
Dynamic power dissipation per package (P)	5 10 15	$1100 f_i + \sum(f_o C_L) \times V_{DD}^2$ $4400 f_i + \sum(f_o C_L) \times V_{DD}^2$ $11\,400 f_i + \sum(f_o C_L) \times V_{DD}^2$	where $f_i$ = input freq. (MHz) $f_o$ = output freq. (MHz) $C_L$ = load capacitance (pF) $\sum(f_o C_L)$ = sum of outputs $V_{DD}$ = supply voltage (V)



**APPLICATION INFORMATION**

An example of application for the HEF4043B is:

- Four-bit storage with output enable