intersil

OBSOLETE PRODUCT
NO RECOMMENDED REPLACEMENT
our Technical Support Center at
1-888-INTERSIL or www.intersil.com/tsc

CA3059, CA3079

Oct 1999

Zero-Voltage Switches for 50Hz-60Hz and 400Hz Thyristor Control Applications

Features

- **Relay Control**
- **Valve Control**
- **Synchronous Switching of Flashing Lights**
- **On-Off Motor Switching**
- **Differential Comparator with Self-Contained Power Supply for Industrial Applications**
- **Photosensitive Control**
- **Power One-Shot Control**
- **Heater Control**
- **Lamp Control**

Type Features

	CA3059	CA3079
24V, 120V, 208/230V, 277V at 50/60 or 400Hz Operation	X	X
Differential Input	X	X
Low Balance Input Current (Max) - μA	1	2
Built-In Protection Circuit for Opened or Shorted Sensor (Term 14)	X	X
Sensor Range (Rx) - kΩ	2 - 100	2 - 50
DC Mode (Term 12)	X	
External Trigger (Term 6)	X	
External Inhibit (Term 1)	X	
DC Supply Volts (Max)	14	10
Operating Temperature Range (°C)	-55 to +125	

Ordering Information

PART NUMBER	TEMPERATURE	PACKAGE
CA3059	-55°C to +125°C	14 Lead Plastic DIP
CA3079	-55°C to +125°C	14 Lead Plastic DIP

Description

The CA3059 and CA3079 zero-voltage switches are monolithic silicon integrated circuits designed to control a thyristor in a variety of AC power switching applications for AC input voltages of 24V, 120V, 208/230V, and 277V at 50Hz-60Hz and 400Hz. Each of the zero-voltage switches incorporates 4 functional blocks (see the Functional Block Diagram) as follows:

1. Limiter-Power Supply - Permits operation directly from an AC line.
2. Differential On/Off Sensing Amplifier - Tests the condition of external sensors or command signals. Hysteresis or proportional-control capability may easily be implemented in this section.
3. Zero-Crossing Detector - Synchronizes the output pulses of the circuit at the time when the AC cycle is at zero voltage point; thereby eliminating radio-frequency interference (RFI) when used with resistive loads.
4. Triac Gating Circuit - Provides high-current pulses to the gate of the power controlling thyristor.

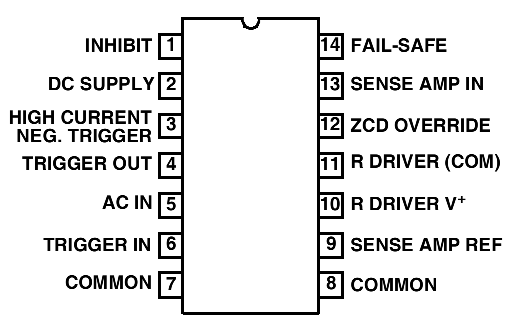
In addition, the CA3059 provides the following important auxiliary functions (see the Functional Block Diagram).

1. A built-in protection circuit that may be actuated to remove drive from the triac if the sensor opens or shorts.
2. Thyristor firing may be inhibited through the action of an internal diode gate connected to Terminal 1.
3. High-power dc comparator operation is provided by overriding the action of the zero-crossing detector. This is accomplished by connecting Terminal 12 to Terminal 7. Gate current to the thyristor is continuous when Terminal 13 is positive with respect to Terminal 9.

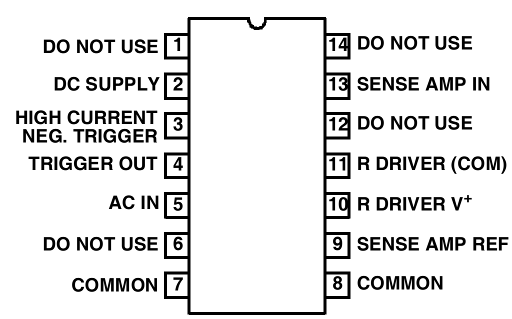
The CA3059 and CA3079 are supplied in 14 lead dual-in-line plastic packages.

Pinouts

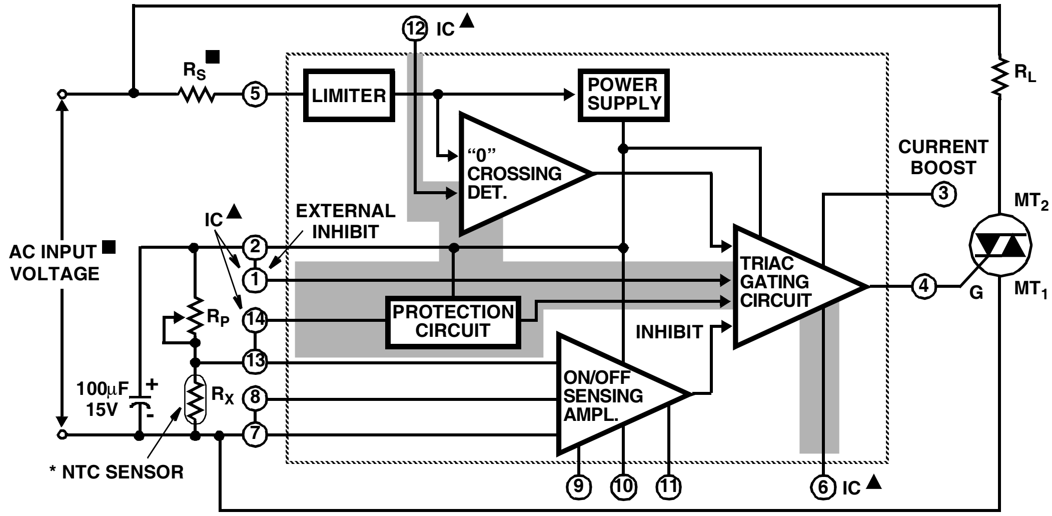
CA3059 (PDIP)
TOP VIEW



CA3079 (PDIP)
TOP VIEW



Functional Block Diagram



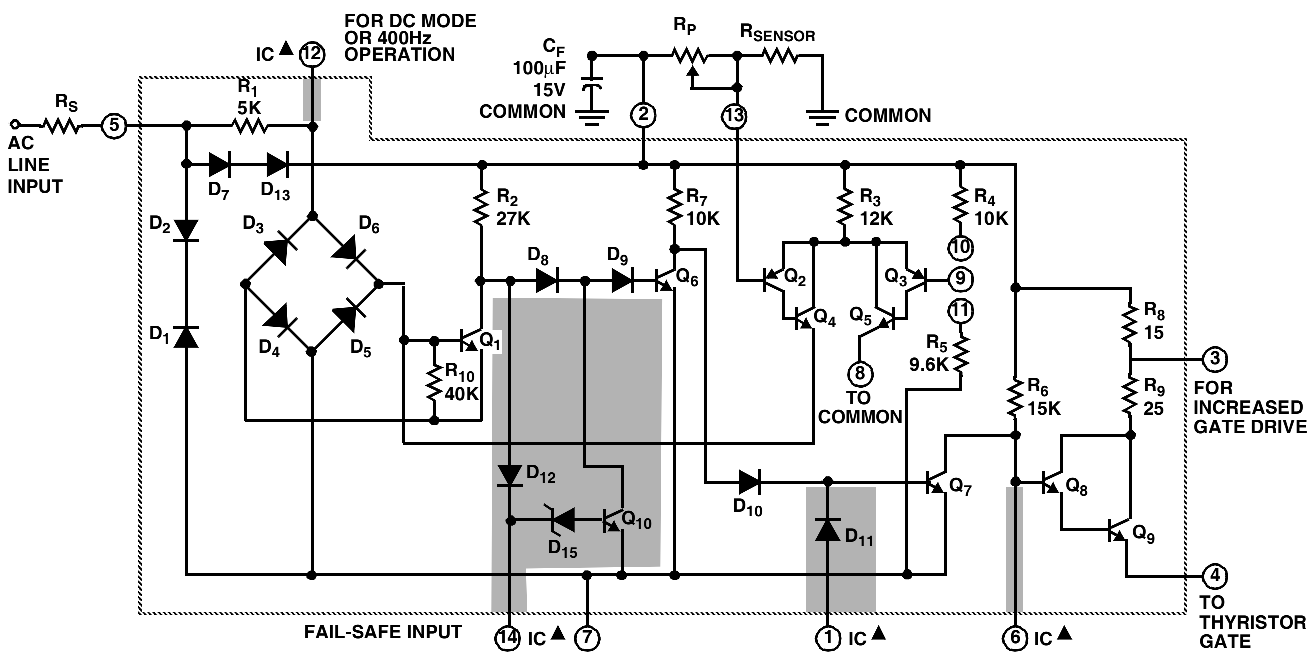
* NEGATIVE TEMPERATURE COEFFICIENT

AC INPUT VOLTAGE (50/60 OR 400Hz) V AC	INPUT SERIES RESISTOR (R_S) kΩ	DISSIPATION RATING FOR R_S W
24	2	0.5
120	10	2
208/230	20	4
277	25	5

NOTE: Circuitry within shaded areas, not included in CA3079

■ See chart

▲ IC = Internal connection - DO NOT USE (Terminal restriction applies only to CA3079)



All resistance values are in Ω

NOTE: Circuitry within shaded areas not included in CA3079

▲ IC = Internal connection - DO NOT USE (Terminal restriction applies only to

FIGURE 1. SCHEMATIC DIAGRAM OF CA3059 AND CA3079

Absolute Maximum Ratings $T_A = +25^oC$

DC Supply Voltage (Between Terminals 2 & 7)
- CA3059 . . . 14V
- CA3079 . . . 10V

DC Supply Voltage (Between Terminals 2 & 8)
- CA3059 . . . 14V
- CA3079 . . . 10V

Peak Supply Current (Terminals 5 & 7) . . . ±50mA
Output Pulse Current (Terminal 4) . . . 150mA

Thermal Information

Thermal Resistance θ_{JA}
- PDIP Package . . . 100°C/W

Power Dissipation
- Up to $T_A = +55^oC$ CA3059, CA3079 . . . 950mW
- Above $T_A = +55^oC$ CA3059, CA3079 . . Derate Linearly 10mW/°C

Ambient Temperature
- Operating . . . -55°C to +125°C
- Storage . . . -65°C to +150°C

Lead Temperature (During Soldering) . . . +265°C
At distance 1/16” ± 1/32” (1.59 ± 0.79) from case for 10 seconds max

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

$T_A = +25^oC$, For all Types, Unless Otherwise Specified. All voltages are measured with respect to Terminal 7. For Operating at $120V_{RMS}$, 50-60Hz (AC Line Voltage) (Note 1)

PARAMETERS		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DC SUPPLY VOLTAGE (Figure 2A, 2B, 2C)							
Inhibit Mode	At 50/60Hz	V_S	$R_S = 8k\Omega$, $I_L = 0$	6.1	6.5	7	V
	At 400Hz		$R_S = 10k\Omega$, $I_L = 0$	-	6.8	-	V
	At 50/60Hz		$R_S = 5k\Omega$, $I_L = 0$	-	6.4	-	V
Pulse Mode	At 50/60Hz	V_S	$R_S = 8k\Omega$, $I_L = 0$	6	6.4	7	V
	At 400Hz		$R_S = 10k\Omega$, $I_L = 0$	-	6.7	-	V
	At 50/60Hz		$R_S = 5k\Omega$, $I_L = 0$	-	6.3	-	V
Gate Trigger Current (Figures 3, 4A)		I_{GT} Terminal 4	Terminals 3 and 2 Connected, $V_{GT} = 1V$	-	105	-	mA
PEAK OUTPUT CURRENT (PULSED) (Figures 4, 5)							
With Internal Power Supply Figure 4a, 4b		I_{OM} Terminal 4	Terminal 3 open, Gate Trigger Voltage (V_{GT}) = 0	50	84	-	mA
			Terminals 3 and 2 Connected, Gate Trigger Voltage (V_{GT}) = 0	90	124	-	mA
With External Power Supply Figure 5a, 5b, 5c		I_{OM} Terminal 4	Terminal 3 open, V+ = 12V, $V_{GT} = 0$	-	170	-	mA
			Terminals 3 and 2 Connected, V+ = 12V, $V_{GT} = 0$		240	-	mA
Inhibit Input Ratio (Figure 6)		V_9/V_2	Voltage Ratio of Terminals 9 to 2	0.465	0.485	0.520	-
TOTAL GATE PULSE DURATION (Note 2) (Figure 7A, 7B, 7C, 7D)							
For Positive dv/dt	50-60Hz	t_P	$C_{EXT} = 0$	70	100	140	µs
	400Hz		$C_{EXT} = 0$, $R_{EXT} = \infty$	-	12	-	µs
For Negative dv/dt	50-60Hz	t_N	$C_{EXT} = 0$	70	100	140	µs
	400Hz		$C_{EXT} = 0$, $R_{EXT} = \infty$	-	10	-	µs
PULSE DURATION AFTER ZERO CROSSING (50-60Hz) (Figure 7A)							
For Positive dv/dt		t_{P1}	$C_{EXT} = 0$, $R_{EXT} = \infty$	-	50	-	µs
For Negative dv/dt		t_{N1}		-	60	-	µs
OUTPUT LEAKAGE CURRENT (Figure 8)							
Inhibit Mode		I_4		-	0.001	10	µA
INPUT BIAS CURRENT (Figure 9)							
CA3059		I_I		-	220	1000	nA
CA3079				-	220	2000	nA
Common-mode Input Voltage Range		V_{CMR}	Terminals 9 and 13 Connected	-	1.5 to 5	-	V

Electrical Specifications $T_A = +25^oC$, For all Types, Unless Otherwise Specified. All voltages are measured with respect to Terminal 7. For Operating at $120V_{RMS}$, 50-60Hz (AC Line Voltage) (Note 1) **(Continued)**

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SENSITIVITY (Note 3) (Figures 4(a), 11)						
Pulse Mode	ΔV_{13}	Terminal 12 open	-	6	-	mV

NOTES:

1. The values given in the Electrical Characteristics Chart at 120V also apply for operation at input voltages of 208/230V, and 277V, except for Pulse Duration. However, the series resistor (R_S) must have the indicated value, shown in the chart in the Functional Block Diagram, for the specified input voltage.
2. Pulse Duration in 50Hz applications is approximately 15% longer than shown in Figure 7(b).
3. Required voltage change at Terminal 13 to either turn OFF the triac when ON or turn ON the triac when OFF.

Maximum Voltage Ratings $T_A = +25^oC$

MAXIMUM VOLTAGE RATINGS $T_A = +25^oC$															MAXIMUM CURRENT RATINGS	
TERM. NO.	NOTE 3 **1**	**2**	**3**	**4**	NOTE 1 **5**	NOTE 3 **6**	**7**	**8**	**9**	**10**	**11**	NOTE 3 **12**	**13**	NOTES 2, 3 **14**	**I_{IN} mA**	**I_{OUT} mA**
1 Note 3		Note 4	Note 4	Note 4	Note 4	15 0	10 -2	Note 4	Note 4	Note 4	Note 4	Note 4	Note 4	Note 4	10	0.1
2			0 -15	0 -15	2 -14	0 -14	0 Note 5 -14	0 Note 5 -14	0 -14	0 -14	0 -14	Note 4	0 -14	0 -14	150	10
3				0 -15	Note 4	Note 4	Note 4	Note 4	Note 4	Note 4	Note 4	Note 4	Note 4	Note 4	Note 4	Note 4
4					Note 4	2 -10	Note 4	Note 4	Note 4	Note 4	Note 4	Note 4	Note 4	Note 4	0.1	150
5 Note 1						Note 4	7 -7	Note 4	Note 4	Note 4	Note 4	Note 4	Note 4	Note 4	50	10
6 Note 3							14 0	Note 4	Note 4	Note 4	Note 4	Note 4	Note 4	Note 4	Note 4	Note 4
7								Note 4	14 0	Note 4	20 0	2.5 -2.5	14 0	6 -6	Note 4	Note 4
8									10 0	Note 4	Note 4	Note 4	Note 4	Note 4	0.1	2
9										Note 4	Note 4	Note 4	Note 4	Note 4	Note 4	Note 4
10											Note 4	Note 4	Note 4	Note 4	Note 4	Note4
11												Note 4	Note 4	Note 4	Note 4	Note4
12 Note 3													Note 4	Note 4	50	50
13														Note 4	Note 4	Note4
14 Note 3															2	2

This chart gives the range of voltages which can be applied to the terminals listed horizontally with respect to the terminals listed vertically. For example, the voltage range of horizontal Terminal 6 to vertical Terminal 4 is 2V to -10V.

NOTES:

1. Resistance should be inserted between Terminal 5 and external supply or line voltage for limiting current into Terminal 5 to less than 50mA.
2. Resistance should be inserted between Terminal 14 and external supply for limiting current into Terminal 14 to less than 2mA.
3. For the CA3079 indicated terminal is internally connected and, therefore, should not be used.
4. Voltages are not normally applied between these terminals; however, voltages appearing between these terminals are safe, if the specified voltage limits between all other terminals are not exceeded.
5. For CA3079 (0V to -10V).

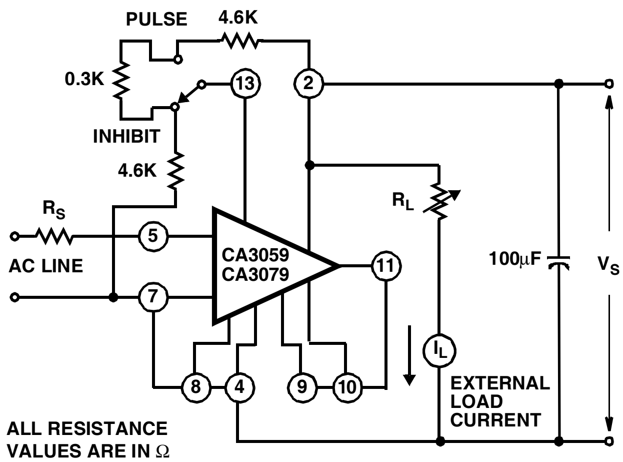


FIGURE 2A. DC SUPPLY VOLTAGE TEST CIRCUIT FOR CA3059 AND CA3079

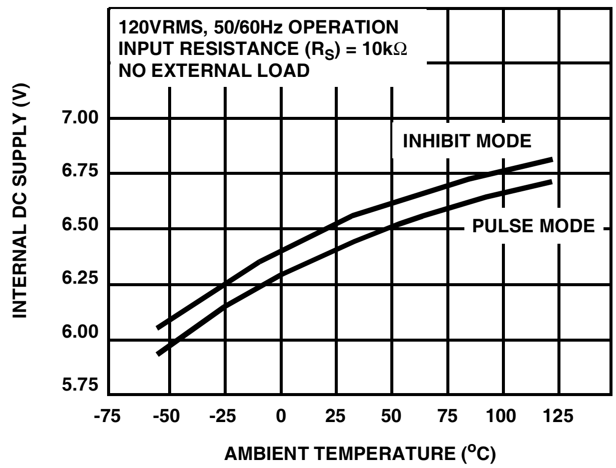


FIGURE 2B. DC SUPPLY VOLTAGE vs AMBIENT TEMPERATURE FOR CA3059 AND CA3079

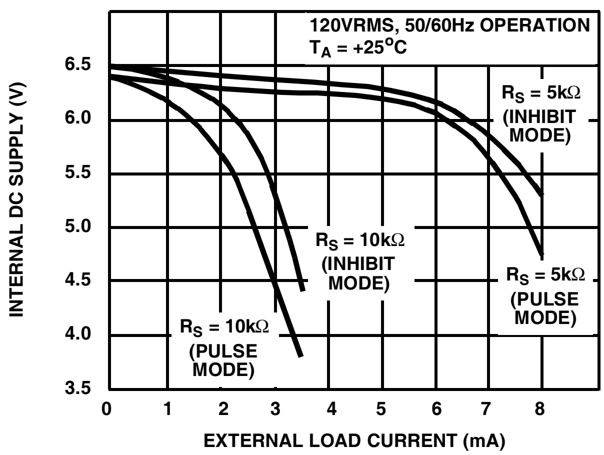


FIGURE 2C. DC SUPPLY VOLTAGE vs EXTERNAL LOAD CURRENT FOR CA3059 AND CA3079

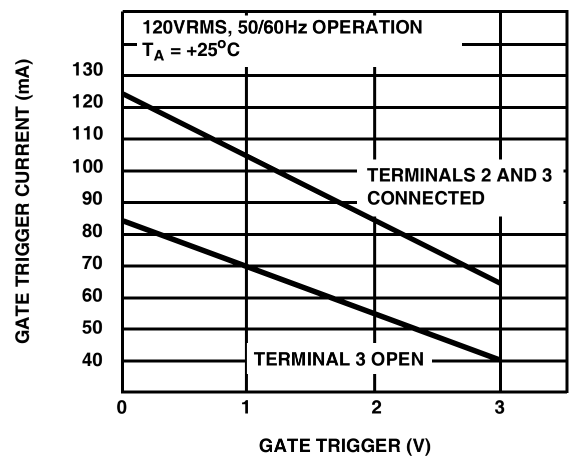


FIGURE 3. GATE TRIGGER CURRENT vs GATE TRIGGER VOLTAGE FOR CA3059 AND CA3079

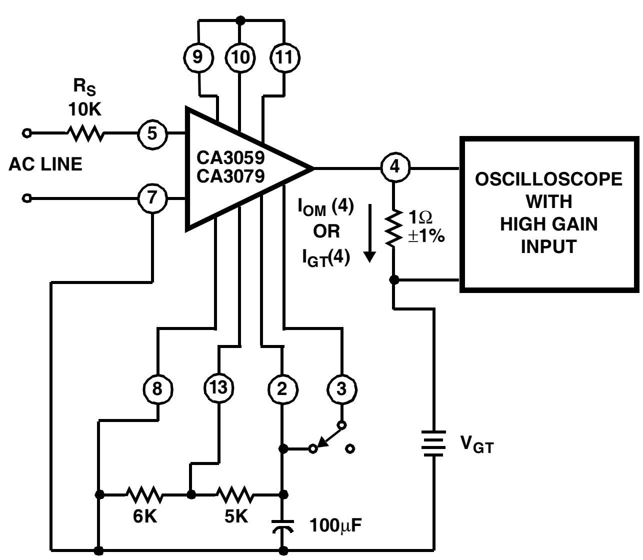


FIGURE 4A. PEAK OUTPUT (PULSED) AND GATE TRIGGER CURRENT WITH INTERNAL POWER SUPPLY TEST CIRCUIT FOR CA3059 AND CA3079

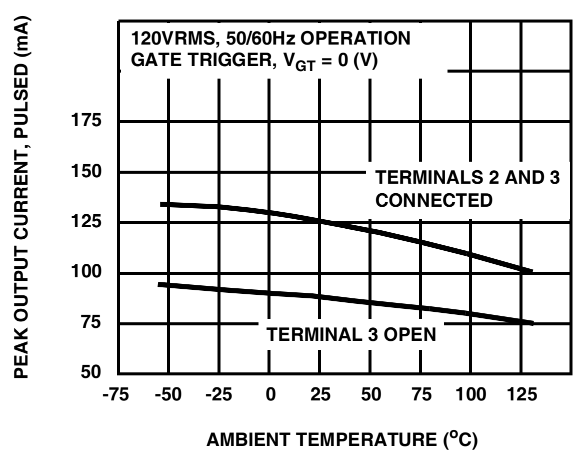


FIGURE 4B. PEAK OUTPUT CURRENT (PULSED) vs AMBIENT TEMPERATURE FOR CA3059 AND CA3079

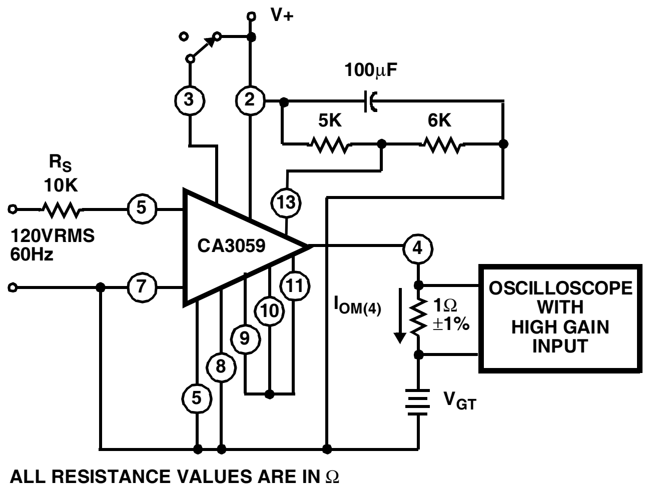


FIGURE 5A. PEAK OUTPUT CURRENT (PULSED) WITH EXTERNAL POWER SUPPLY TEST CIRCUIT FOR CA3059

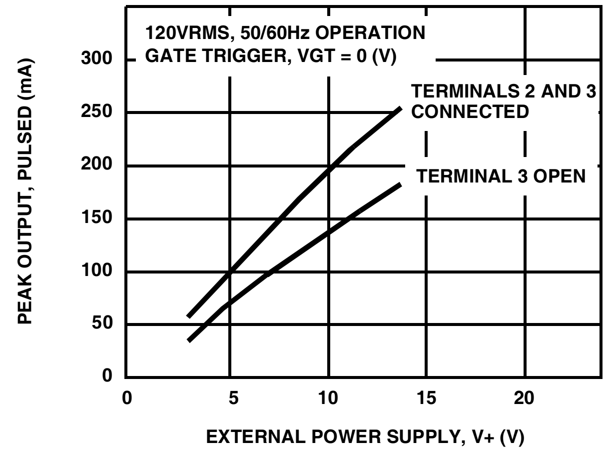


FIGURE 5B. PEAK OUTPUT CURRENT (PULSED) vs EXTERNAL POWER SUPPLY VOLTAGE FOR CA3059

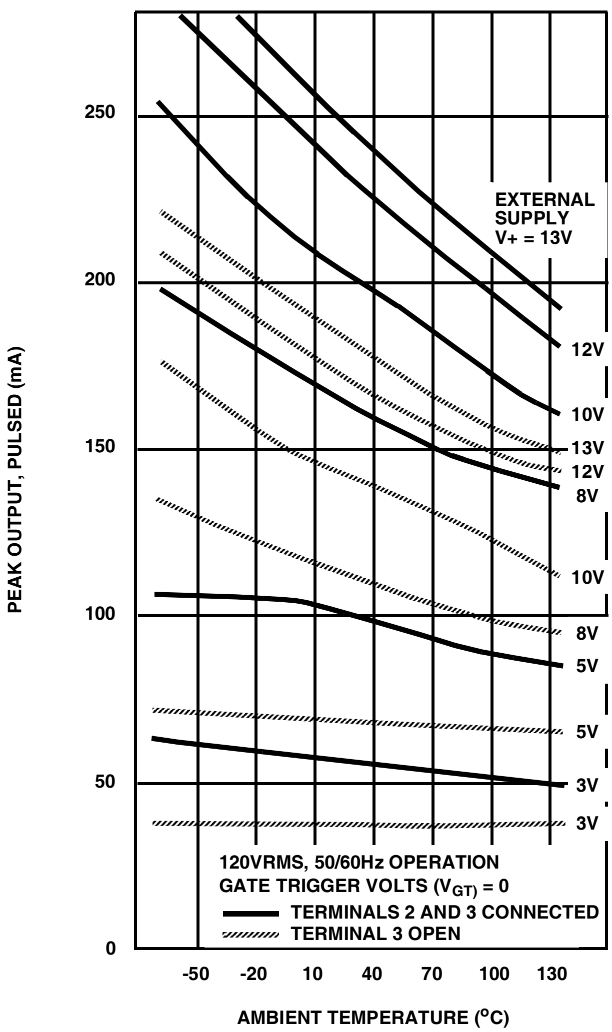


FIGURE 5C. PEAK OUTPUT CURRENT (PULSED) vs AMBIENT TEMPERATURE FOR CA3059

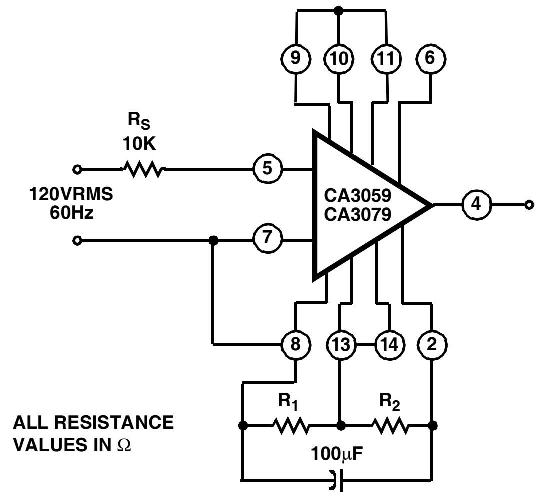


FIGURE 6(A). INPUT INHIBIT VOLTAGE RATIO TEST CIRCUIT FOR CA3059 AND CA3079

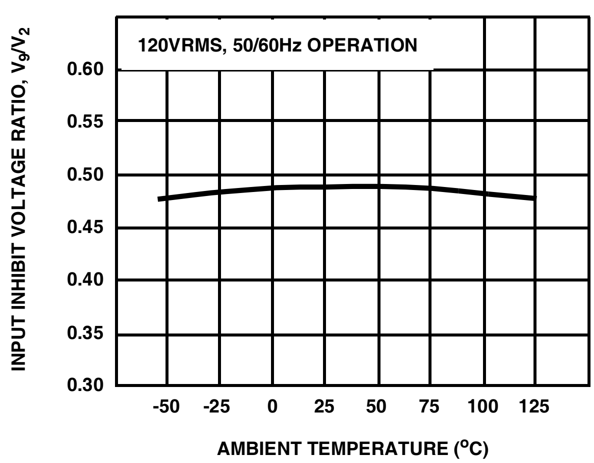
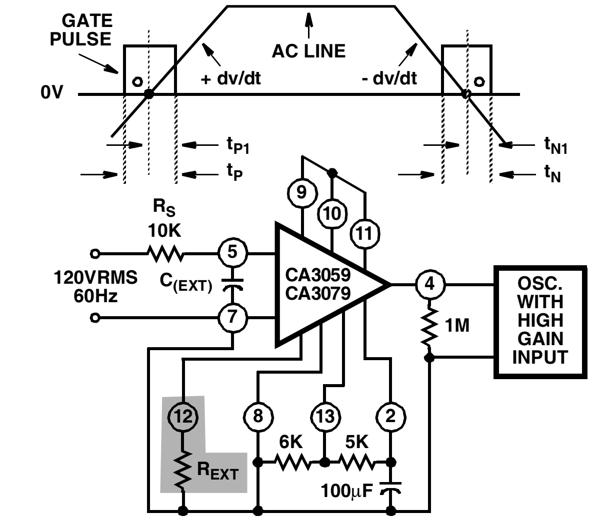


FIGURE 6B. INPUT INHIBIT VOLTAGE RATIO vs AMBIENT TEMPERATURE FOR CA3059 AND CA3079



NOTE: Circuitry within shaded area not included in CA3079.
All resistance values are in Ω

FIGURE 7A. GATE PULSE DURATION TEST CIRCUIT WITH ASSOCIATED WAVEFORM FOR CA3059 AND CA3079

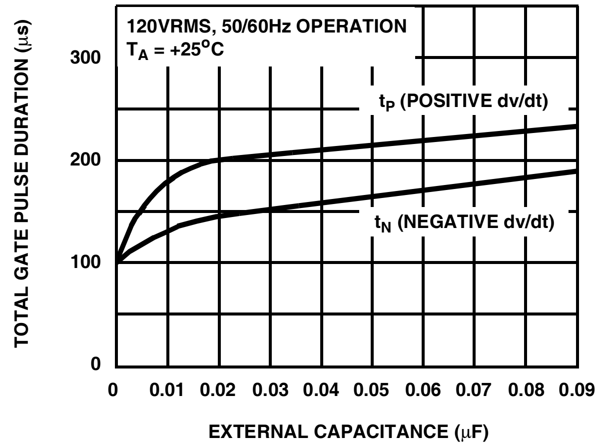


FIGURE 7B. TOTAL GATE PULSE DURATION vs EXTERNAL CAPACITANCE FOR CA3059 AND CA3079

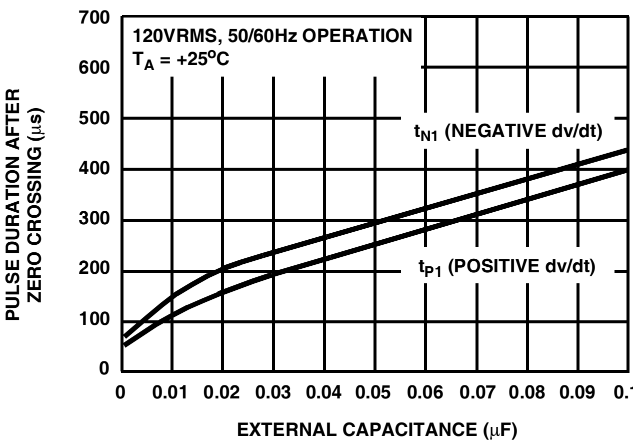


FIGURE 7C. PULSE DURATION AFTER ZERO CROSSING vs EXTERNAL CAPACITANCE FOR CA3059 & CA3079

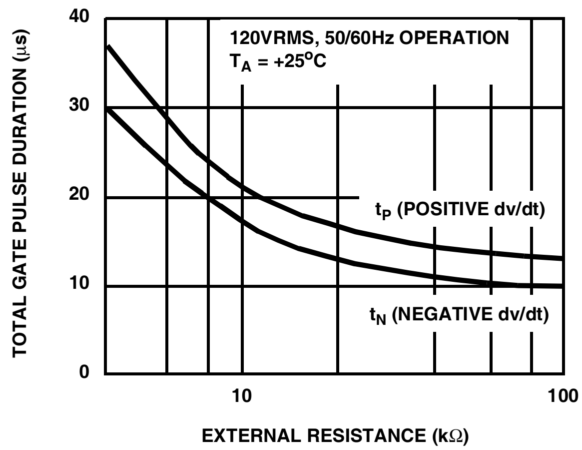


FIGURE 7D. TOTAL GATE PULSE DURATION vs EXTERNAL RESISTANCE FOR CA3059

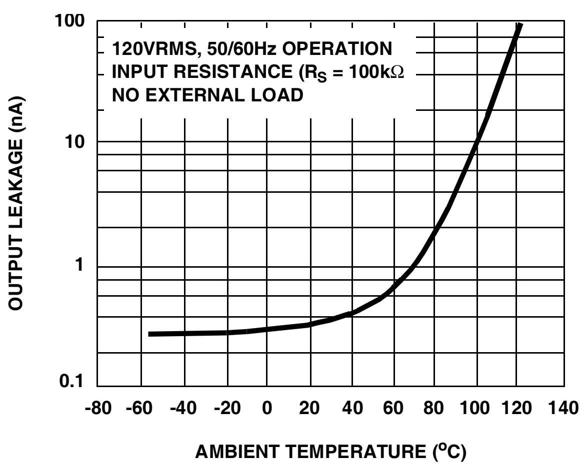


FIGURE 8. OUTPUT LEAKAGE CURRENT (INHIBIT MODE) vs AMBIENT TEMPERATURE FOR CA3059 AND CA3079

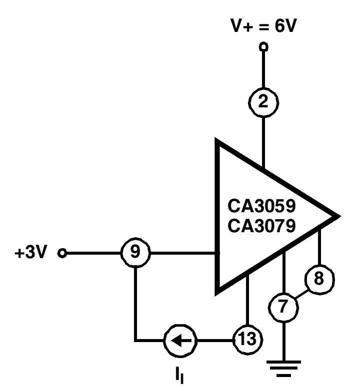


FIGURE 9. INPUT BIAS CURRENT TEST CIRCUIT FOR CA3059 AND CA3079

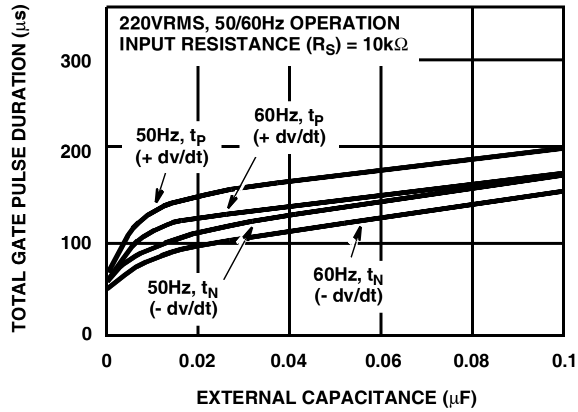


FIGURE 10A.

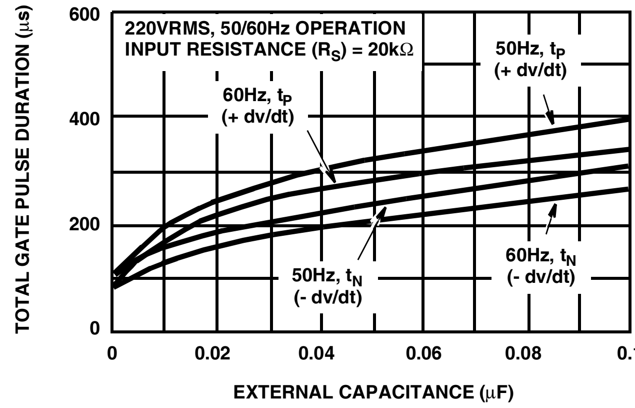


FIGURE 10B.

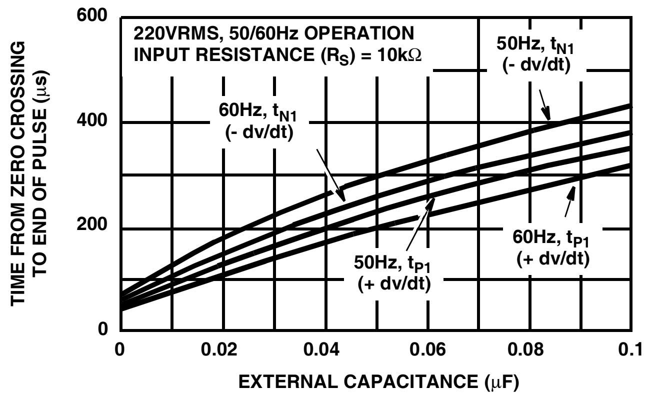


FIGURE 10C.

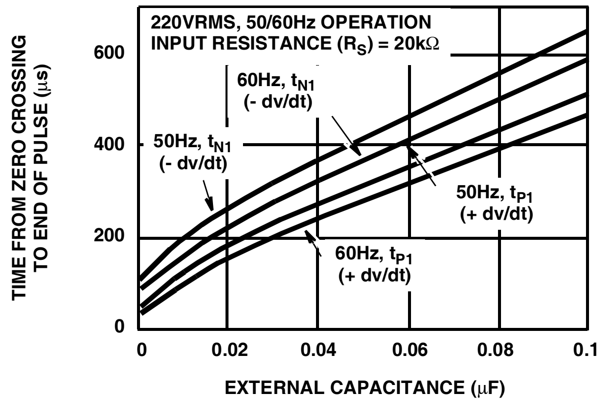


FIGURE 10D.

FIGURE 10. RELATIVE PULSE WIDTH AND LOCATION OF ZERO CROSSING FOR 220V OPERATION FOR CA3059 AND CA3079

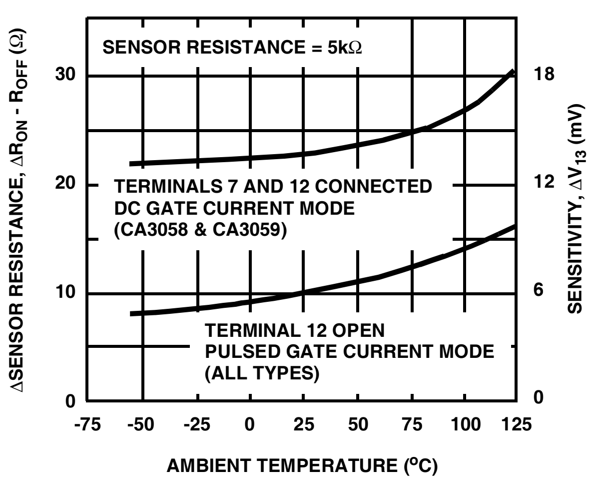


FIGURE 11. SENSITIVITY vs AMBIENT TEMPERATURE FOR CA3059 AND CA3079

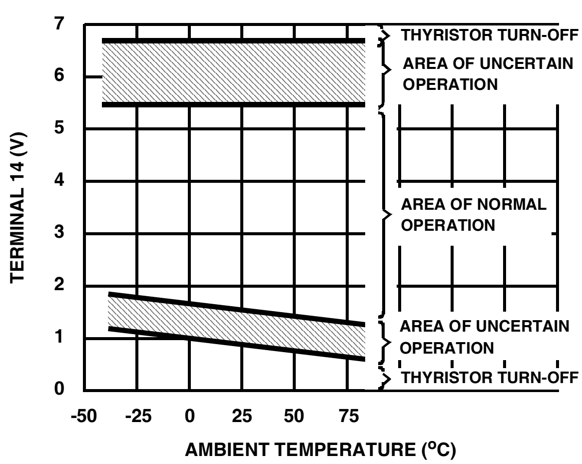
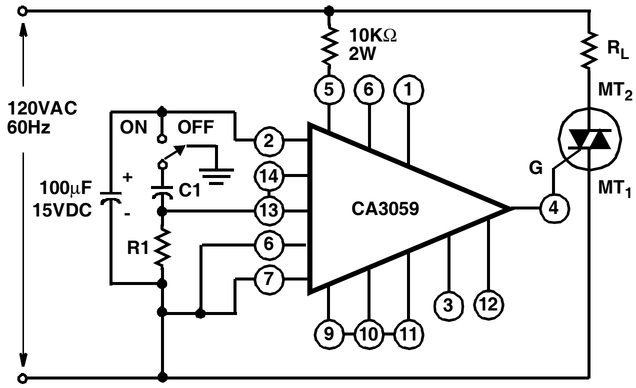


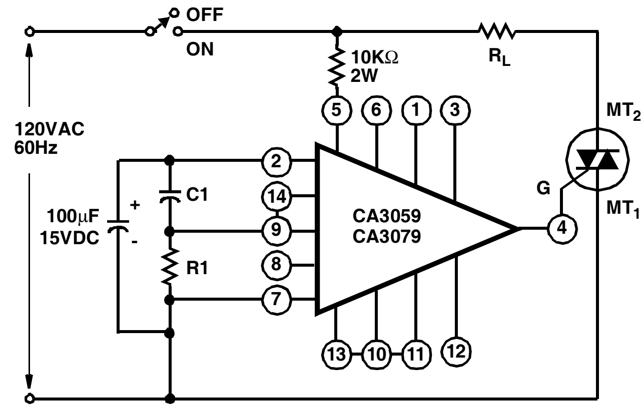
FIGURE 12. OPERATING REGIONS FOR BUILT-IN PROTECTION CIRCUIT FOR CA3059



$t_{ON} = 0.67\ R_1C_1$

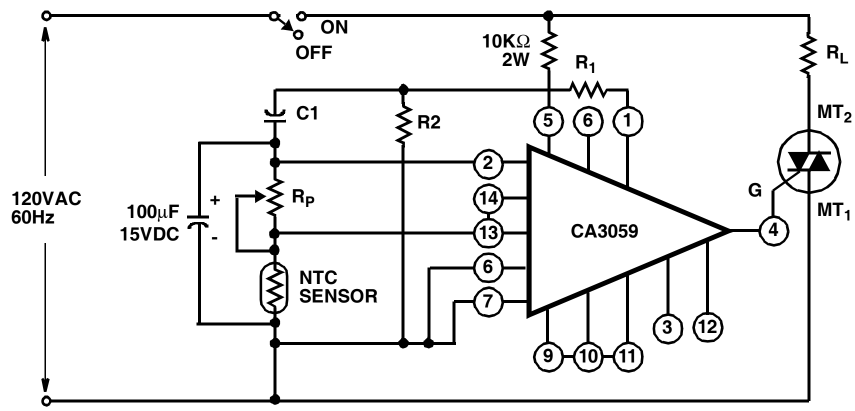
R_1(max. value allowable) = 1mΩ

FIGURE 13. LINE-OPERATED ONE-SHOT TIMER



$t_d = 0.67\ R_1C_1$

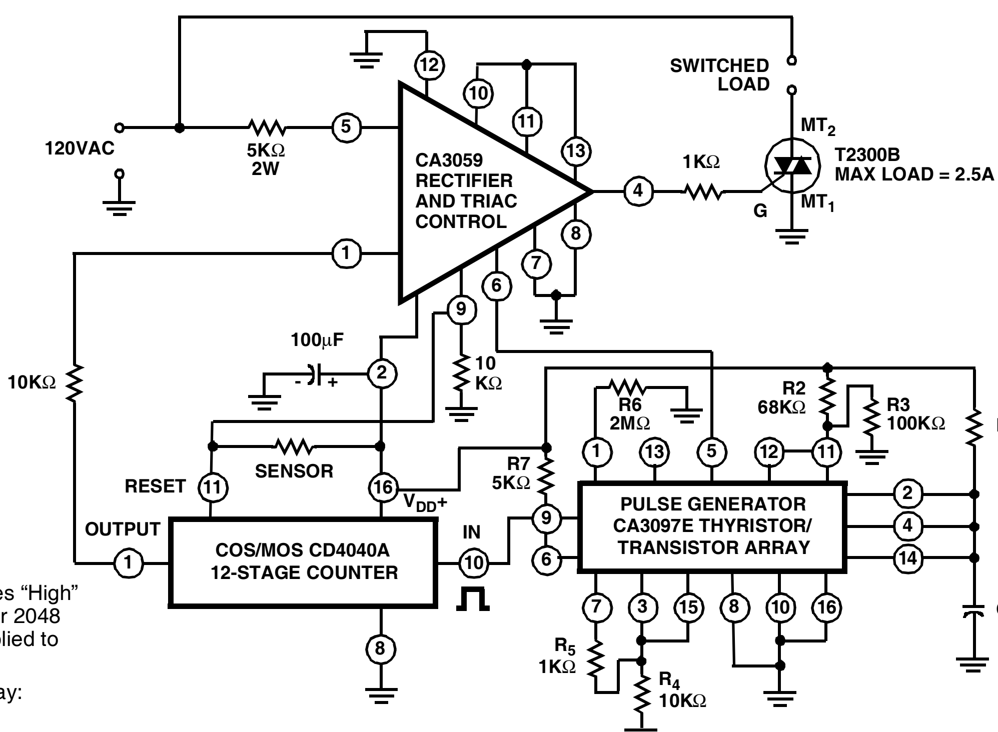
FIGURE 14. LINE-OPERATED THYRISTOR CONTROL TIME DELAY TURN-ON CIRCUIT



$t_d = R_TC_1$

$$R_T = \frac{R_1R_2}{R_1 + R_2}$$

FIGURE 15. ON/OFF TEMPERATURE CONTROL CIRCUIT WITH DELAYED TURN-ON



NOTE:

Terminal 1 goes “High” (Logic “1”) after 2048 pulses are applied to Terminal 10.

For 8 hour delay:
R_1 = 12MΩ
C_1 = 2µF

FIGURE 16A. LINE-OPERATED IC TIMER FOR LONG TIME PERIODS

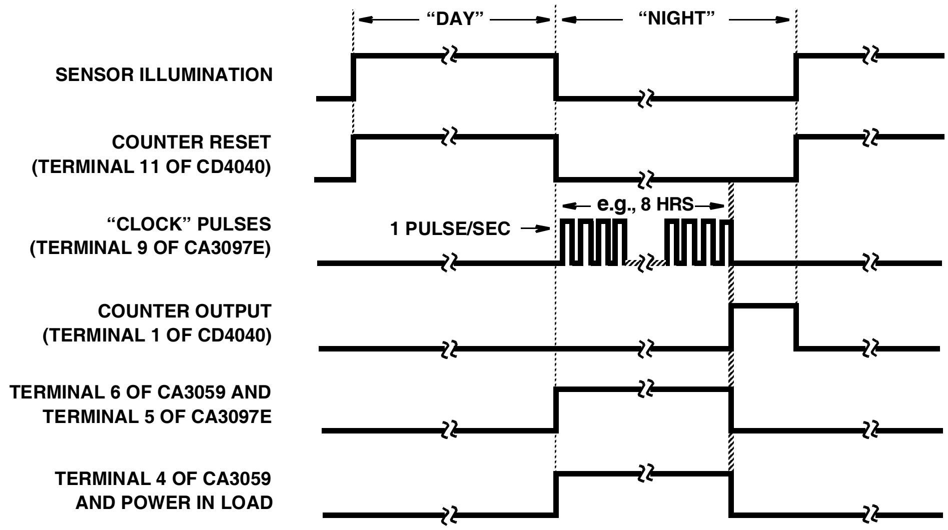


FIGURE 16B. TIMING DIAGRAM FOR FIGURE 16A

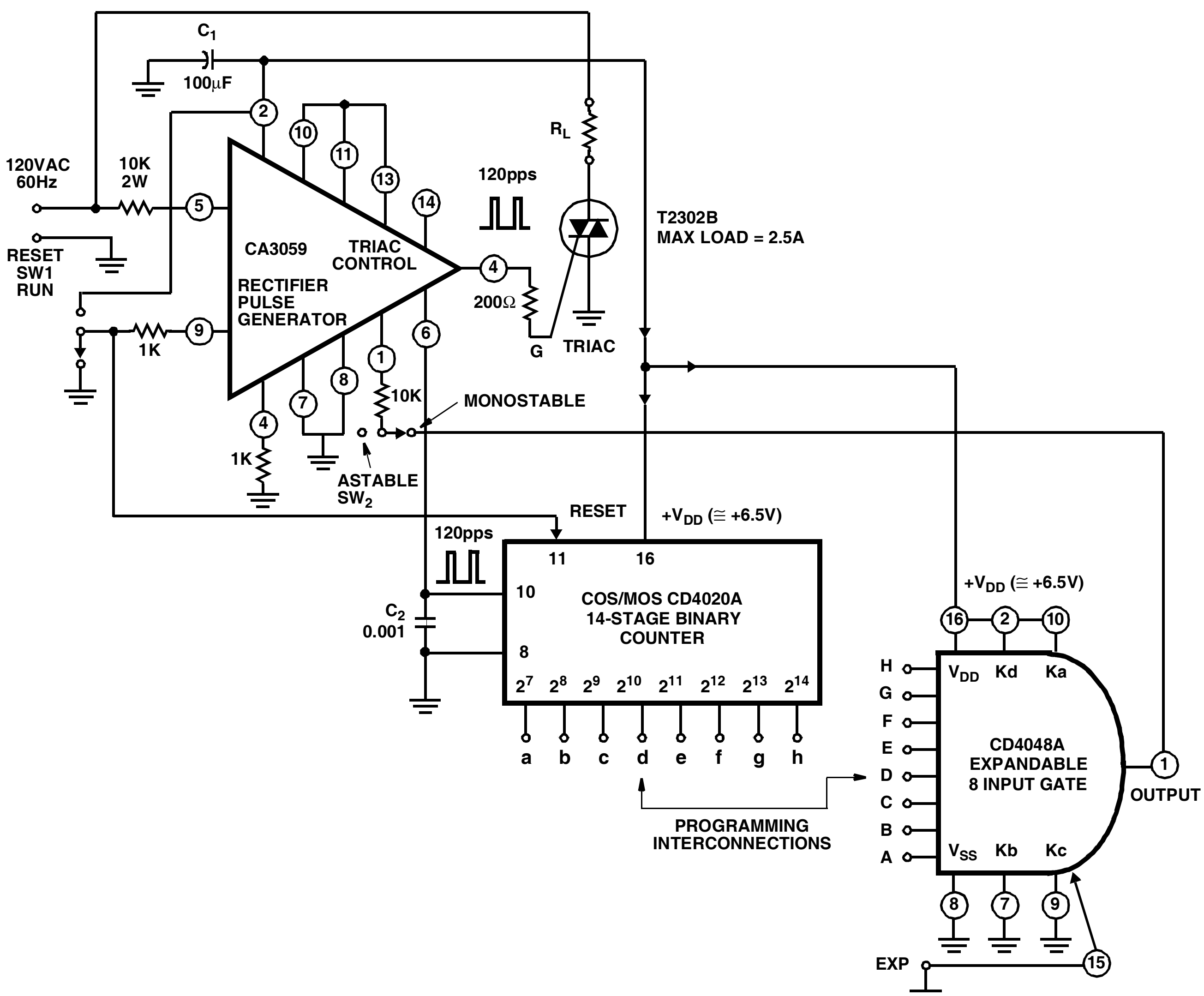


FIGURE 17A. PROGRAMMABLE ULTRA-ACCURATE LINE-OPERATED TIMER.

TIME PERIODS (t = 0.5333 s)								
1t	2t	4t	8t	16t	32t	64t	128t	t_O
CD4020A TERMINALS								
a	b	c	d	e	f	g	h	
CD4048A TERMINALS								
A	B	C	D	E	F	G	H	
C	NC	NC	NC	NC	NC	NC	NC	1t
NC	C	NC	NC	NC	NC	NC	NC	2t
C	C	NC	NC	NC	NC	NC	NC	3t
NC	NC	C	NC	NC	NC	NC	NC	4t
C	NC	C	NC	NC	NC	NC	NC	5t
NC	C	C	NC	NC	NC	NC	NC	6t
C	C	C	NC	NC	NC	NC	NC	7t
NC	NC	NC	C	NC	NC	NC	NC	8t
C	NC	NC	C	NC	NC	NC	NC	9t
NC	C	NC	C	NC	NC	NC	NC	10t
C	C	NC	C	NC	NC	NC	NC	11t
NC	NC	C	C	NC	NC	NC	NC	12t
C	NC	C	C	NC	NC	NC	NC	13t
NC	C	C	C	NC	NC	NC	NC	14t
C	C	C	C	NC	NC	NC	NC	15t
C	C	C	C	NC	C	C	NC	111t
NC	NC	NC	NC	C	C	C	NC	112t
C	NC	NC	NC	C	C	C	NC	113t
C	C	C	C	C	C	C	C	255t

NOTES:

1. t_O = Total time delay = n_1 t + n_2 t + . . . n_nt.
2. C = Connect. For example, interconnect terminal a of the CD4020A and terminal A of the CD4048A.
3. NC = No Connection. For example, terminal b of the CD4020A open and terminal B of the CD4048A connected to $+V_{DD}$ bus.

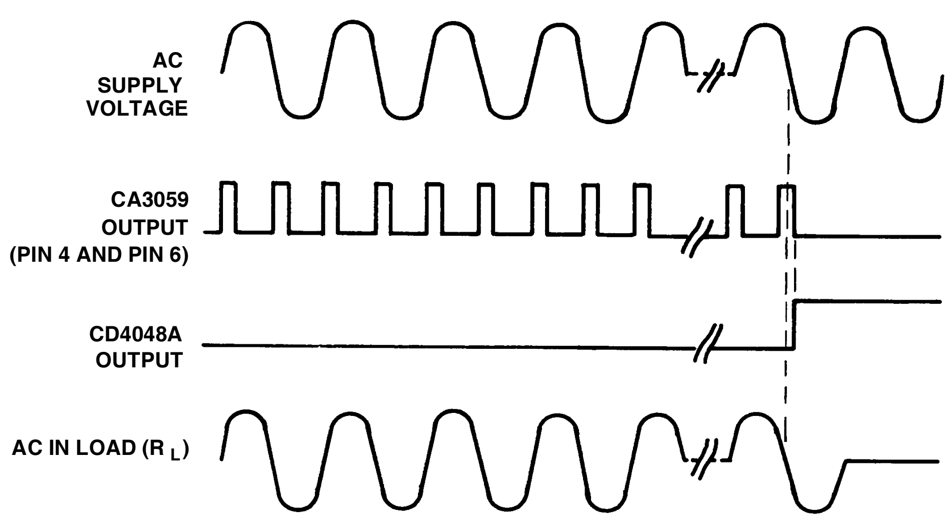


FIGURE 17B. "PROGRAMMING" TABLE FOR FIGURE 17(A).

Operating Considerations

Power Supply Considerations for CA3059 and CA3079

The CA3059 and CA3079 are intended for operation as self-powered circuits with the power supplied from and AC line through a dropping resistor. The internal supply is designed to allow for some current to be drawn by the auxiliary power circuits. Typical power supply characteristics are given in Figures 2(b) and 2(c).

Power Supply Considerations for CA3059

The output current available from the internal supply may not be adequate for higher power applications. In such applications an external power supply with a higher voltage should be used with a resulting increase in the output level. (See Figure 4 for the peak output current characteristics.) When an external power supply is used, Terminal 5 should be connected to Terminal 7 and the synchronizing voltage applied to Terminal 12 as illustrated in Figure 5(a).

Operation of Built-In Protection for the CA3059

A special feature of the CA3059 is the inclusion of a protection circuit which, when connected, removes power from the load if the sensor either shorts or opens. The protection circuit is activated by connecting Terminal 14 to Terminal 13 as shown in the Functional Block Diagram. To assure proper operation of the protection circuit the following conditions should be observed:

1. Use the internal supply and limit the external load current to 2mA with a 5kΩ dropping resistor.
2. Set the value of R_P and sensor resistance (R_X) between 2kΩ and 100kΩ.
3. The ratio of R_X to R_P, typically, should be greater than 0.33 and less than 3. If either of these ratios is not met with an unmodified sensor over the entire anticipated temperature range, then either a series or shunt resistor must be added to avoid undesired activation of the circuit.

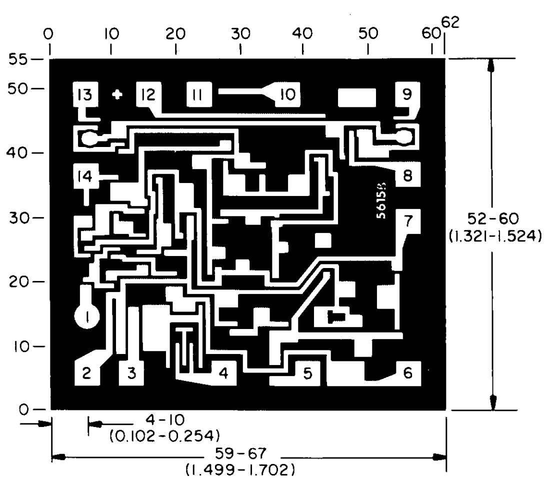
If operation of the protection circuit is desired under conditions other than those specified above, then apply the data given in Figure 12.

External Inhibit Function for the CA3059

A priority inhibit command may be applied to Terminal 1. The presence of at least +1.2V at 10μA will remove drive from the thyristor. This required level is compatible with DTL or T^2L logic. A logical 1 activates the inhibit function.

DC Gate Current Mode for the CA3059

Connecting Terminals 7 and 12 disables the zero-crossing detector and permits the flow of gate current on demand from the differential sensing amplifier. This mode of operation is useful when comparator operation is desired or when inductive loads are switched. Care must be exercised to avoid overloading the internal power supply when operating in this mode. A sensitive gate thyristor should be used with a resistor placed between Terminal 4 and the gate in order to limit the gate current.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid gradations are in mils (10^{-3} inch).

The photographs and dimensions represent a chip when it is par of the wafer. When the wafer is cut into chips, the cleavage angles are 57^o instead of 90^o with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17mm) larger in both dimensions.