



**N-Channel Enhancement-Mode Vertical DMOS FETs**

**Ordering Information**

BV <sub>DSS</sub> / BV <sub>DGS</sub>	R <sub>DS(ON)</sub> (max)	I <sub>D(ON)</sub> (min)	Order Number / Package
			TO-92
120V	6.0Ω	1.0A	VN1206L

**Features**

- Free from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low C<sub>ISS</sub> and fast switching speeds
- Excellent thermal stability
- Integral Source-Drain diode
- High input impedance and high gain
- Complementary N- and P-channel devices

**Applications**

- Motor controls
- Converters
- Amplifiers
- Switches
- Power supply circuits
- Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

**Absolute Maximum Ratings**

Drain-to-Source Voltage	BV <sub>DSS</sub>
Drain-to-Gate Voltage	BV <sub>DGS</sub>
Gate-to-Source Voltage	± 30V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

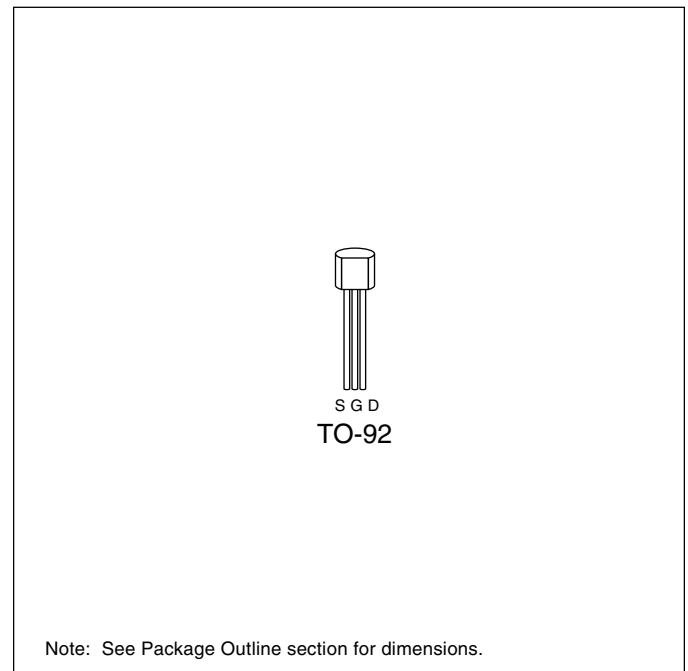
\* Distance of 1.6 mm from case for 10 seconds.

**Advanced DMOS Technology**

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

**Package Option**



## Thermal Characteristics

Package	$I_D$ (continuous)*	$I_D$ (pulsed)	Power Dissipation @ $T_C = 25^\circ\text{C}$	$\theta_{jC}$ $^\circ\text{C/W}$	$\theta_{jA}$ $^\circ\text{C/W}$	$I_{DR}^*$	$I_{DRM}$
TO-92	0.23A	2.0A	1W	125	170	0.23A	2.0A

\*  $I_D$  (continuous) is limited by max rated  $T_j$ .

## Electrical Characteristics (@ $25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
$BV_{DSS}$	Drain-to-Source Breakdown Voltage	120			V	$V_{GS} = 0V, I_D = 100\mu\text{A}$
$V_{GS(th)}$	Gate Threshold Voltage	0.8		2.0	V	$V_{GS} = V_{DS}, I_D = 1\text{mA}$
$I_{GSS}$	Gate Body Leakage			100	nA	$V_{GS} = \pm 15V, V_{DS} = 0V$
$I_{DSS}$	Zero Gate Voltage Drain Current			10	$\mu\text{A}$	$V_{GS} = 0V, V_{DS} = \text{Max Rating}$
				500		$V_{GS} = 0V, V_{DS} = \text{Max Rating}$ $T_A = 125^\circ\text{C}$
$I_{D(ON)}$	ON-State Drain Current	1.0			A	$V_{GS} = 10V, V_{DS} = 10V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			10	$\Omega$	$V_{GS} = 2.5V, I_D = 0.1\text{A}$
				6.0		$V_{GS} = 10V, I_D = 0.5\text{A}$
$G_{FS}$	Forward Transconductance	300			$\text{m}\Omega^{-1}$	$V_{DS} = 10V, I_D = 0.5\text{A}$
$C_{ISS}$	Input Capacitance			125	$\text{pF}$	$V_{GS} = 0V, V_{DS} = 25V$ $f = 1\text{MHz}$
$C_{OSS}$	Common Source Output Capacitance			50		
$C_{RSS}$	Reverse Transfer Capacitance			20		
$t_r$	Rise Time			8.0	ns	$V_{DD} = 60V, I_D = 0.4\text{A}$ $R_{GEN} = 25\Omega$
$t_{d(ON)}$	Turn-ON Delay Time			8.0		
$t_f$	Fall Time			12		
$t_{d(OFF)}$	Turn-OFF Delay Time			18		
$V_{SD}$	Diode Forward Voltage Drop		1.2		V	$I_{SD} = 0.25\text{A}, V_{GS} = 0V$

### Notes:

- All D.C. parameters 100% tested at  $25^\circ\text{C}$  unless otherwise stated. (Pulse test: 300 $\mu\text{s}$  pulse, 2% duty cycle.)
- All A.C. parameters sample tested.

## Switching Waveforms and Test Circuit

