

# DATA SHEET

**74F378**

Hex D flip-flop with enable

Product specification

1989 Oct 05

IC15 Data Handbook

Hex D flip-flop with enable

74F378

FEATURES

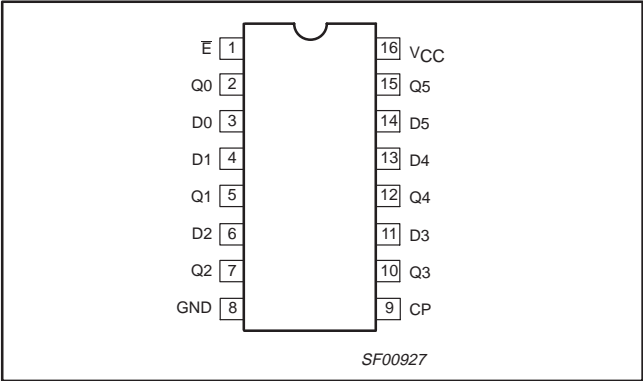
- 6-bit high-speed parallel register
- Positive edge-triggered D-type inputs
- Fully buffered common Clock and Enable inputs
- Input clamp diodes limit high speed termination effects
- Fully TTL and CMOS compatible

DESCRIPTION

The 74F378 has six edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously when the Enable (E) input is Low.

The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition is transformed to the corresponding flop-flop's Q output. The E input must be stable one setup time prior to the Low-to-High clock transition for predictable operation.

PIN CONFIGURATION



TYPE	TYPICAL $f_{max}$	TYPICAL SUPPLY CURRENT (TOTAL)
74F378	100MHz	35mA

ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$ , $T_{amb} = 0^{\circ}C \text{ to } +70^{\circ}C$	PKG DWG #
16-pin plastic DIP	N74F378N	SOT38-4
16-pin plastic SO	N74F378D	SOT109-1

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

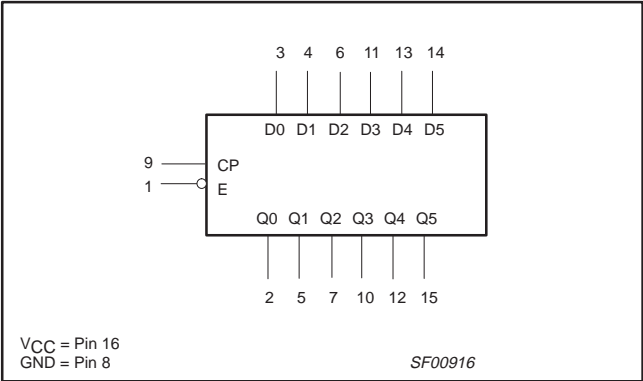
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 – D5	Data inputs	1.0/1.0	20μA/0.6mA
CP	Clock pulse input (active rising edge)	1.0/1.0	20μA/0.6mA
E	Enable input (active low)	1.0/1.0	20μA/0.6mA
Q0 – Q5	Data outputs	50/33	1.0mA/20mA

**NOTE:**  
One (1.0) FAST unit load is defined as: 20μA in the High state and 0.6mA in the Low state.

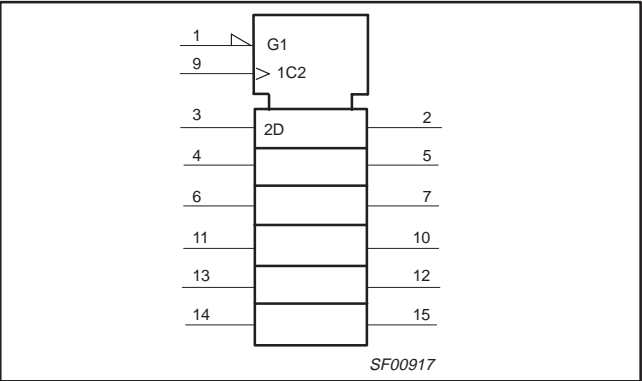
Hex D flip-flop with enable

74F378

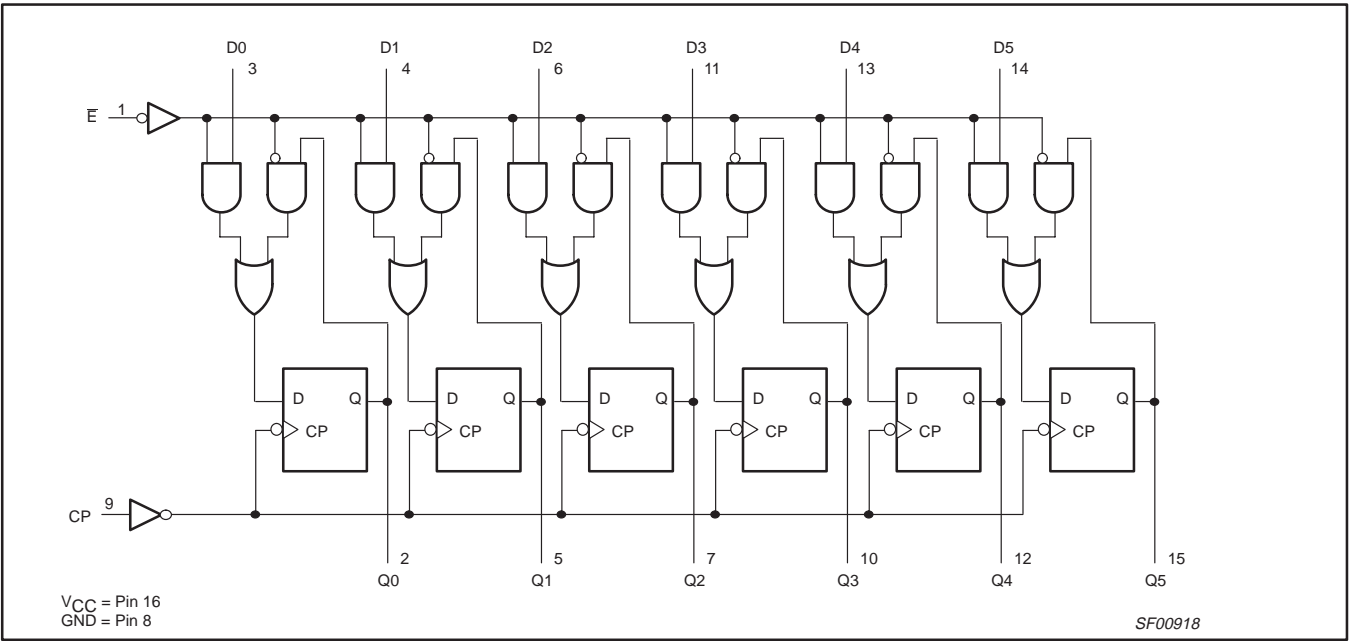
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUTS	OPERATING MODE
$\bar{E}$	CP	D <sub>n</sub>	Q <sub>n</sub>	
l	↑	h	H	Load "1"
l	↑	l	L	Load "0"
h H	↑ X	X X	no change no change	Hold (do nothing)

H = High-voltage level  
h = High-voltage level one setup time prior to the Low-to-High clock transition  
L = Low-voltage level  
l = Low-voltage level one setup time prior to the Low-to-High clock transition  
X = Don't care  
↑ = Low-to-High clock transition

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74F378

**ABSOLUTE MAXIMUM RATINGS**

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
$V_{CC}$	Supply voltage	-0.5 to +7.0	V
$V_{IN}$	Input voltage	-0.5 to +7.0	V
$I_{IN}$	Input current	-30 to +5	mA
$V_{OUT}$	Voltage applied to output in High output state	-0.5 to $V_{CC}$	V
$I_{OUT}$	Current applied to output in Low output state	40	mA
$T_{amb}$	Operating free-air temperature range	0 to +70	°C
$T_{stg}$	Storage temperature range	-65 to +150	°C

**RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER SYMBOL	LIMITS			UNIT
		MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5.0	5.5	V
$V_{IH}$	High-level input voltage	2.0			V
$V_{IL}$	Low-level input voltage			0.8	V
$I_{IK}$	Input clamp current			-18	mA
$I_{OH}$	High-level output current			-1	mA
$I_{OL}$	Low-level output current			20	mA
$T_{amb}$	Operating free-air temperature range	0		70	°C

**DC ELECTRICAL CHARACTERISTICS**

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS <sup>1</sup>		LIMITS			UNIT
					MIN	TYP <sup>2</sup>	MAX	
V <sub>OH</sub>	High-level output voltage		V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN, I <sub>OH</sub> = MAX	±10%V <sub>CC</sub>	2.5			V
				±5%V <sub>CC</sub>	2.7	3.4		V
V <sub>OL</sub>	Low-level output voltage		V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN, I <sub>OL</sub> = MAX	±10%V <sub>CC</sub>		0.30	0.50	V
				±5%V <sub>CC</sub>		0.30	0.50	V
V <sub>IK</sub>	Input clamp voltage		V <sub>CC</sub> = MIN, I <sub>I</sub> = I <sub>IK</sub>			−0.73	−1.2	V
I <sub>I</sub>	Input current at maximum input voltage		V <sub>CC</sub> = MAX, V <sub>I</sub> = 7.0V				100	μA
I <sub>IH</sub>	High-level input current		V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7V				20	μA
I <sub>IL</sub>	Low-level input current		V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5V				−0.6	mA
I <sub>OS</sub>	Short-circuit output current <sup>3</sup>		V <sub>CC</sub> = MAX		−60		−150	mA
I <sub>CC</sub>	Supply current (total)	I <sub>CC</sub> H	V <sub>CC</sub> = MAX			32	45	mA
		I <sub>CC</sub> L				35	45	mA

**Notes:**

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at  $V_{CC} = 5\text{V}$ ,  $T_{amb} = 25^\circ\text{C}$ .
- Not more than one output should be shorted at a time. For testing  $I_{OS}$ , the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests,  $I_{OS}$  tests should be performed last.

## Hex D flip-flop with enable

74F378

## AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T <sub>amb</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω			T <sub>amb</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V ± 10% C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f <sub>MAX</sub>	Maximum clock frequency	Waveform 1	80	100		80		MHz
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay CP to Qn	Waveform 1	3.0 3.5	5.5 6.0	7.5 8.5	3.0 3.5	8.5 9.5	ns

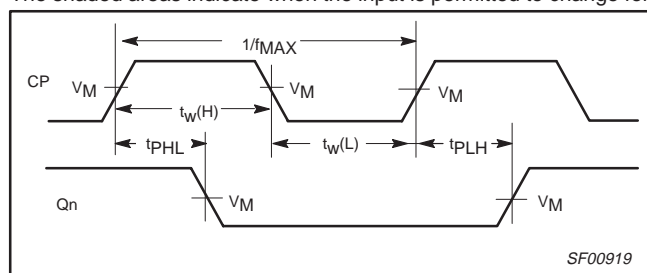
## AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T <sub>amb</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω			T <sub>amb</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V ± 10% C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω			
			MIN	TYP	MAX	MIN	MAX		
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup time, High or Low Dn to CP	Waveform 2	4.0 4.0			4.0 4.0		ns	
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold time, High or Low Dn to CP	Waveform 2	0 0			0 0		ns	
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup time, High or Low E to CP	Waveform 2	4.0 10.0			4.0 10.0		ns	
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold time, High or Low E to CP	Waveform 2	0 0			0 0		ns	
t <sub>w</sub> (H) t <sub>w</sub> (L)	CP Pulse width, High or Low	Waveform 1	4.0 6.0			4.0 6.0		ns	

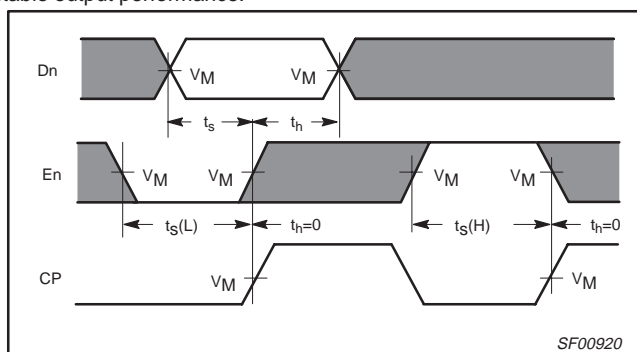
## AC WAVEFORMS

For all waveforms, V<sub>M</sub> = 1.5V.

The shaded areas indicate when the input is permitted to change for predictable output performance.



Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency

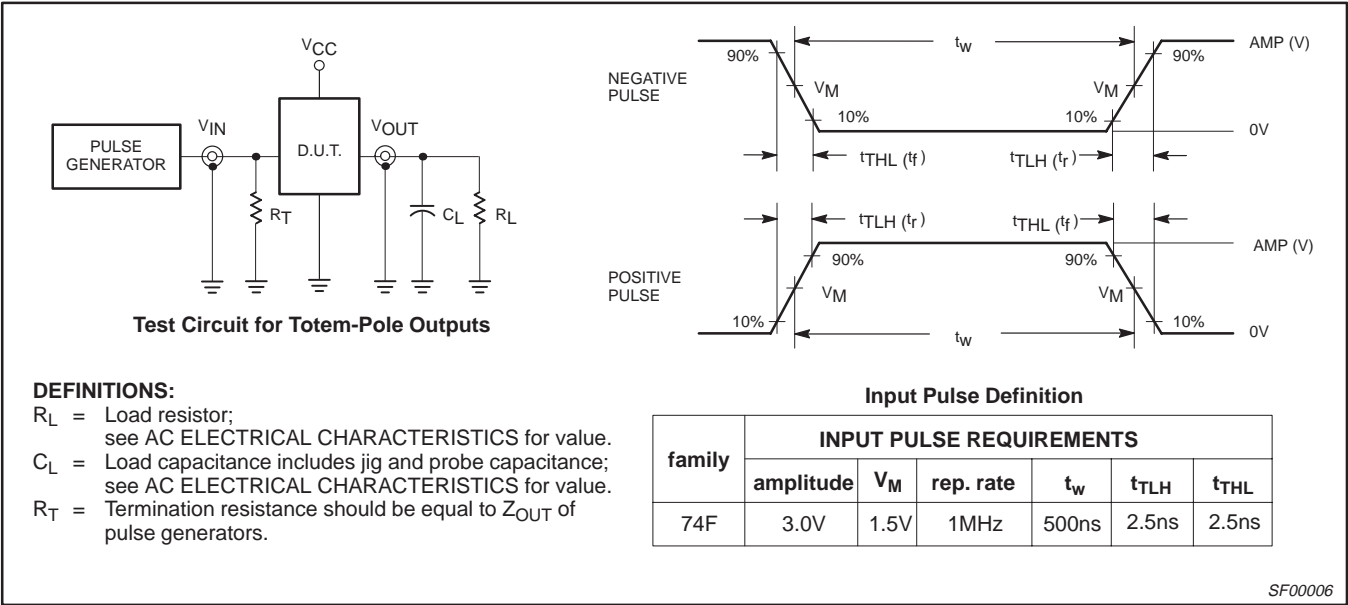


Waveform 2. Data and Enable Setup Time and Hold Times

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74F378

TEST CIRCUIT AND WAVEFORM

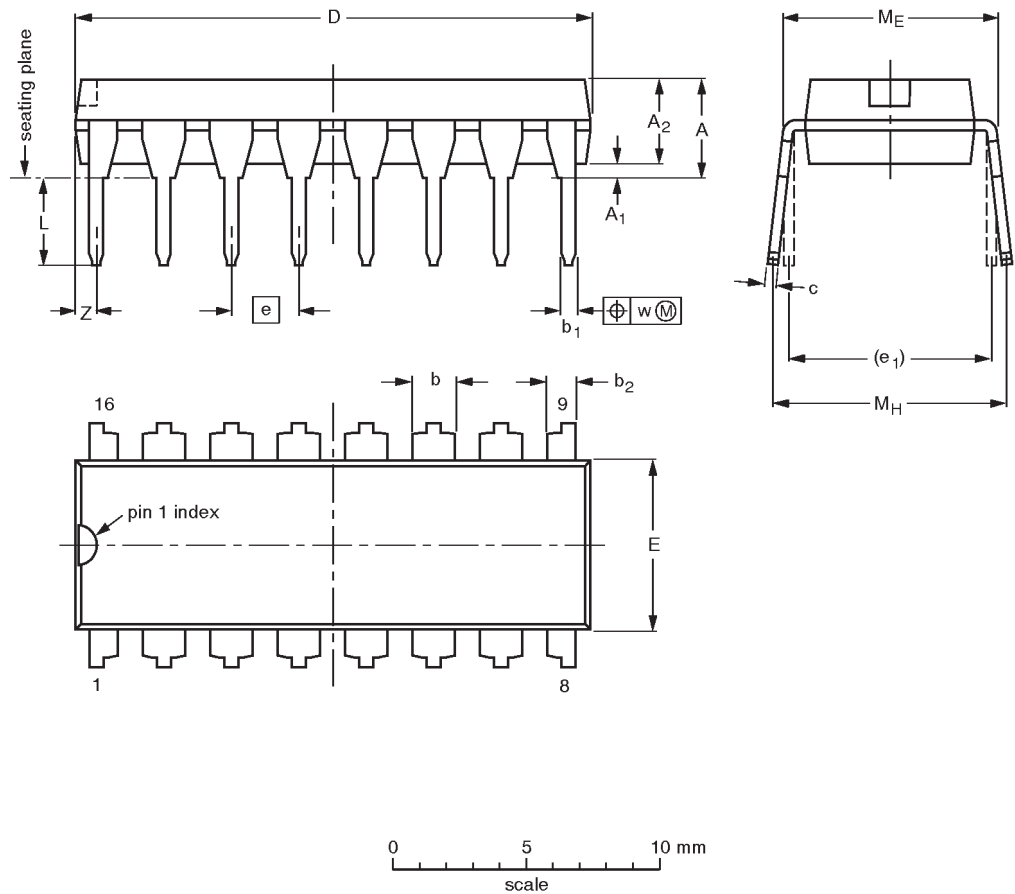


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74F378

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	b <sub>2</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

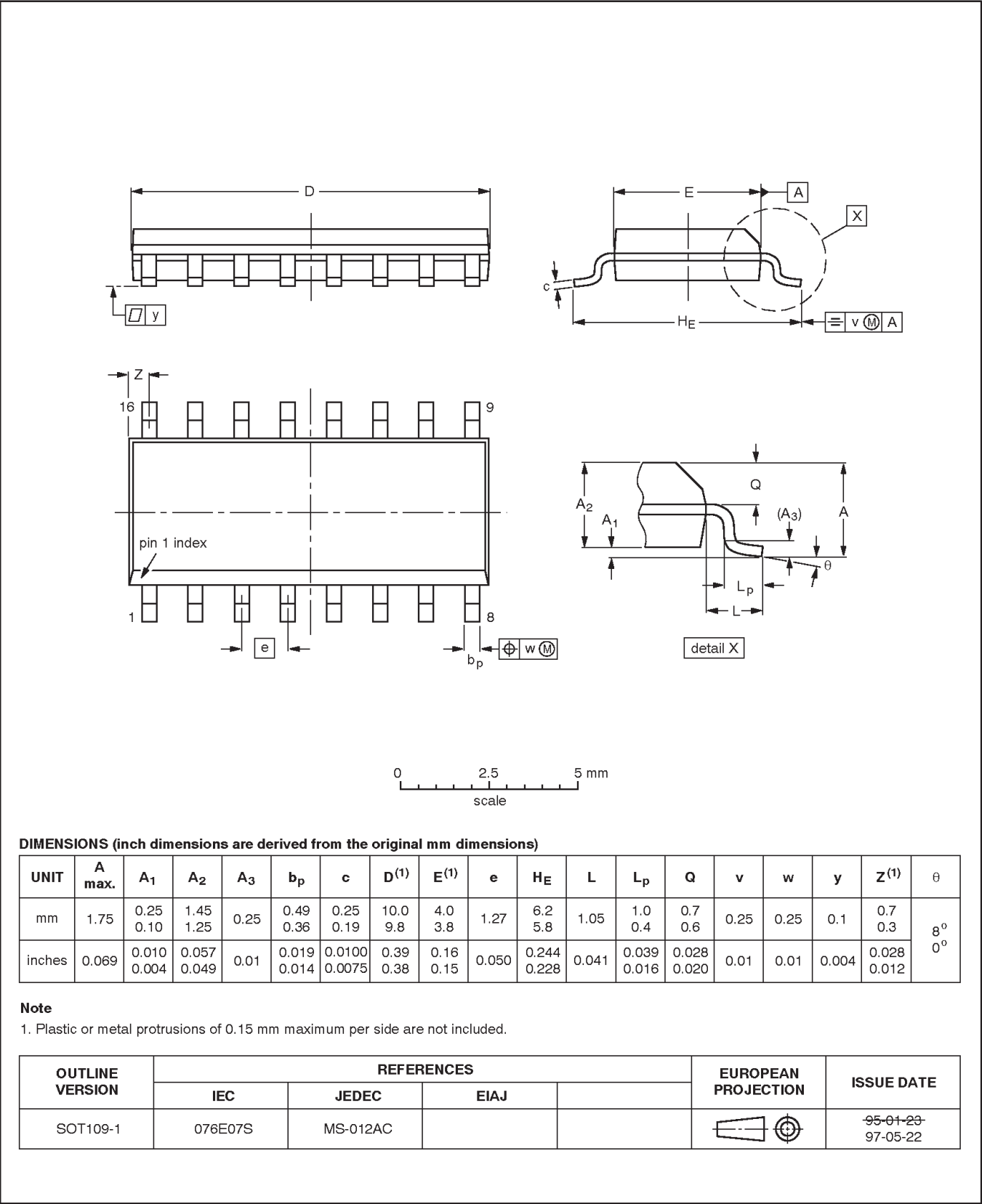
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						92-11-17 95-01-14

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74F378

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1





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74F378

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**NOTES**

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74F378

## Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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