Appendix A - Atmel ATmega88/168 Automotive Specification at 150°C

DATASHEET

Description

This document contains information specific to devices operating at temperatures up to 150°C. Only deviations are covered in this appendix, all other information can be found in the complete Automotive datasheet. The complete Automotive datasheet can be found on http://www.atmel.com

1. Electrical Characteristics

1.1 Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Test Conditions	Unit
Operating temperature	–55 to +150	°C
Storage temperature	–65 to +175	°C
Voltage on any pin except $\overline{\text{RESET}}$ with respect to ground	–0.5 to V_{CC}+0.5	V
Voltage on $\overline{\text{RESET}}$ with respect to ground	–0.5 to +13.0	V
Maximum operating voltage	6.0	V
DC current per I/O pin DC current V_{CC} and GND	30 200.0	mA

1.2 DC Characteristics

T_A = –40°C to +150°C, V_{CC} = 2.7V to 5.5V (unless otherwise noted)

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Input low voltage, except XTAL1 and $\overline{\text{RESET}}$ pin	V_{CC} = 2.7V to 5.5V	V_{IL}	–0.5		$+0.3V_{CC}$ (1)	V
Input high voltage, except XTAL1 and $\overline{\text{RESET}}$ pins	V_{CC} = 2.7V to 5.5V	V_{IH}	$0.6V_{CC}$ (2)		V_{CC} + 0.5	V
Input low voltage, XTAL1 pin	V_{CC} = 2.7V to 5.5V	V_{IL1}	–0.5		$+0.1V_{CC}$ (2)	V
Input high voltage, XTAL1 pin	V_{CC} = 2.7V to 5.5V	V_{IH1}	$0.7V_{CC}$ (2)		V_{CC} + 0.5	V
Input low voltage, $\overline{\text{RESET}}$ pin	V_{CC} = 2.7V to 5.5V	V_{IL2}	–0.5		$+0.2V_{CC}$ (1)	V
Input high voltage, $\overline{\text{RESET}}$ pin	V_{CC} = 2.7V to 5.5V	V_{IH2}	$0.9V_{CC}$ (2)		V_{CC} + 0.5	V

Notes:
1. “Max” means the highest value where the pin is guaranteed to be read as low
2. “Min” means the lowest value where the pin is guaranteed to be read as high
3. Although each I/O port can sink more than the test conditions (20mA at V_{CC} = 5V) under steady state conditions (non-transient), the following must be observed:
   1] The sum of all IOL, for all ports, should not exceed 400mA.
   2] The sum of all IOL, for ports C0 - C5, should not exceed 200mA.
   3] The sum of all IOL, for ports C6, D0 - D4, should not exceed 300mA.
   4] The sum of all IOL, for ports B0 - B7, D5 - D7, should not exceed 300mA.
   If IOL exceeds the test condition, VOL may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test condition.
4. Although each I/O port can source more than the test conditions (20mA at V_{CC} = 5V) under steady state conditions (non-transient), the following must be observed:
   1] The sum of all IOH, for all ports, should not exceed 400mA.
   2] The sum of all IOH, for ports C0 - C5, should not exceed 200mA.
   3] The sum of all IOH, for ports C6, D0 - D4, should not exceed 300mA.
   4] The sum of all IOH, for ports B0 - B7, D5 - D7, should not exceed 300mA.
   If IOH exceeds the test condition, VOH may exceed the related specification. Pins are not guaranteed to source current greater than the listed test condition.
5. Minimum V_{CC} for Power-down is 2.5V

1.2 DC Characteristics (Continued)

T_A = –40°C to +150°C, V_{CC} = 2.7V to 5.5V (unless otherwise noted)

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Input low voltage, RESET pin as I/O	V_{CC} = 2.7V to 5.5V	V_{IL3}	–0.5		$+0.3V_{CC}$ (1)	V
Input high voltage, RESET pin as I/O	V_{CC} = 2.7V to 5.5V	V_{IH3}	$0.6V_{CC}$ (2)		V_{CC} + 0.5	V
Output low voltage (3), I/O pin except RESET	I_{OL} = 20mA, V_{CC} = 5V I_{OL} = 5mA, V_{CC} = 3V	V_{OL}			0.8 0.5	V
Output high voltage (4) I/O pin except RESET	I_{OH} = –20mA, V_{CC} = 5V I_{OH} = –10mA, V_{CC} = 3V	V_{OH}	4.0 2.2			V
Input leakage current I/O pin	V_{CC} = 5.5V, pin low (absolute value)	I_{IL}			1	µA
Input leakage current I/O pin	V_{CC} = 5.5V, pin high (absolute value)	I_{IH}			1	µA
Reset pull-up resistor		R_{RST}	30		60	kΩ
I/O pin pull-up resistor		R_{PU}	20		50	kΩ
Power supply current (5)	Active 4MHz, V_{CC} = 3V Active 8MHz, V_{CC} = 5V	I_{CC}			8 16	mA
	Active 16MHz, V_{CC} = 5V	$I_{CC\ IDLE}$			25	mA
	Idle 4MHz, V_{CC} = 3V Idle 8MHz, V_{CC} = 5V				6 12	mA
	Idle 16MHz, V_{CC} = 5V				14	mA
Power-down mode	WDT enabled, V_{CC} = 3V WDT enabled, V_{CC} = 5V	$I_{CC\ PWD}$			90 140	µA
	WDT disabled, V_{CC} = 3V WDT disabled, V_{CC} = 5V				80 120	µA
Analog comparator input offset voltage	V_{CC} = 5V V_{in} = V_{CC}/2	V_{ACIO}		< 10	40	mV
Analog comparator input leakage current	V_{CC} = 5V V_{in} = V_{CC}/2	I_{ACLK}	–50		+50	nA
Analog comparator propagation delay	V_{CC} = 4.0V	t_{ACPD}		500		ns

Notes:
1. “Max” means the highest value where the pin is guaranteed to be read as low
2. “Min” means the lowest value where the pin is guaranteed to be read as high
3. Although each I/O port can sink more than the test conditions (20mA at V_{CC} = 5V) under steady state conditions (non-transient), the following must be observed:
   1] The sum of all IOL, for all ports, should not exceed 400mA.
   2] The sum of all IOL, for ports C0 - C5, should not exceed 200mA.
   3] The sum of all IOL, for ports C6, D0 - D4, should not exceed 300mA.
   4] The sum of all IOL, for ports B0 - B7, D5 - D7, should not exceed 300mA.
   If IOL exceeds the test condition, VOL may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test condition.
4. Although each I/O port can source more than the test conditions (20mA at V_{CC} = 5V) under steady state conditions (non-transient), the following must be observed:
   1] The sum of all IOH, for all ports, should not exceed 400mA.
   2] The sum of all IOH, for ports C0 - C5, should not exceed 200mA.
   3] The sum of all IOH, for ports C6, D0 - D4, should not exceed 300mA.
   4] The sum of all IOH, for ports B0 - B7, D5 - D7, should not exceed 300mA.
   If IOH exceeds the test condition, VOH may exceed the related specification. Pins are not guaranteed to source current greater than the listed test condition.
5. Minimum V_{CC} for Power-down is 2.5V

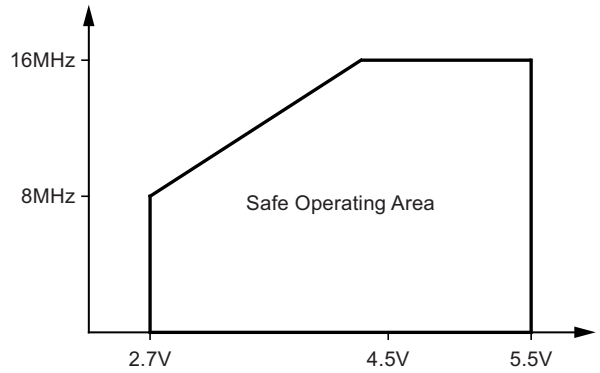
1.3 Memory Endurance

EEPROM endurance: 50,000 write/erase cycles.
Flash endurance: 10,000 write/erase cycles.

1.4 Maximum Speed versus V_{CC}

Maximum frequency is dependent on V_{CC}. As shown in Figure 1-1, the maximum frequency versus V_{CC} curve is linear between $2.7V < V_{CC} < 4.5V$.

Figure 1-1. Maximum Frequency versus V_{CC}



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1.5 ADC Characteristics(1)

T_A = –40°C to +150°C, V_{CC} = 4.5V to 5.5V (unless otherwise noted)

Parameters	Test Conditions	Symbol	Min	Typ	Max	Unit
Resolution				10		Bits
Absolute accuracy (including INL, DNL, quantization error, gain and offset error)	V_{REF} = 4V, V_{CC} = 4V, ADC clock = 200kHz			2	3.5	LSB
	V_{REF} = 4V, V_{CC} = 4V, ADC clock = 200kHz Noise reduction mode			2	3.5	LSB
Integral non-linearity (INL)	V_{REF} = 4V, V_{CC} = 4V, ADC clock = 200kHz			0.6	2.5	LSB
Differential non-linearity (DNL)	V_{REF} = 4V, V_{CC} = 4V, ADC clock = 200kHz			0.30	1.0	LSB
Gain error	V_{REF} = 4V, V_{CC} = 4V, ADC clock = 200kHz		–3.5	–1.3	+3.5	LSB
Offset error	V_{REF} = 4V, V_{CC} = 4V, ADC clock = 200kHz			1.8	3.5	LSB
Conversion time	Free running conversion		13 cycles			µs
Clock frequency			50		200	kHz
Analog supply voltage		AV_{CC}	V_{CC} – 0.3		V_{CC} + 0.3	V
Reference voltage		V_{REF}	1.0		AV_{CC}	V
Input voltage		V_{IN}	GND		V_{REF}	V
Input bandwidth				38.5		kHz
Internal voltage reference		V_{INT}	1.0	1.1	1.2	V
Reference input resistance		R_{REF}	25.6	32	38.4	kΩ
Analog input resistance		R_{AIN}		100		MΩ

Note: 1. Based on standard voltage range (2.7V to 5.5V) characterization results. To be confirmed after actual silicon characterization.

2. ATmega88/168 Typical Characteristics

2.1 Active Supply Current

Figure 2-1. Active Supply Current versus Frequency (1MHz to 20MHz)

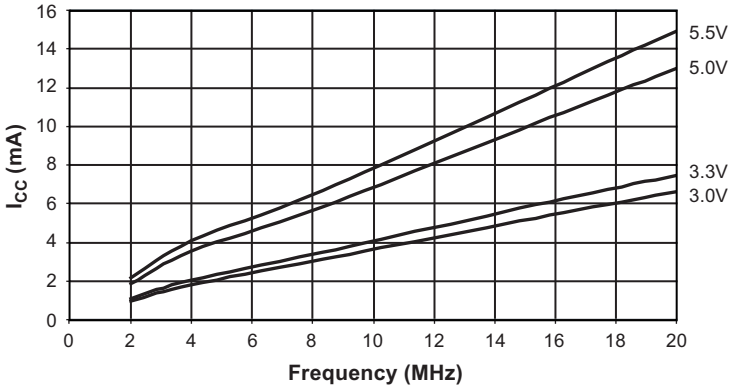
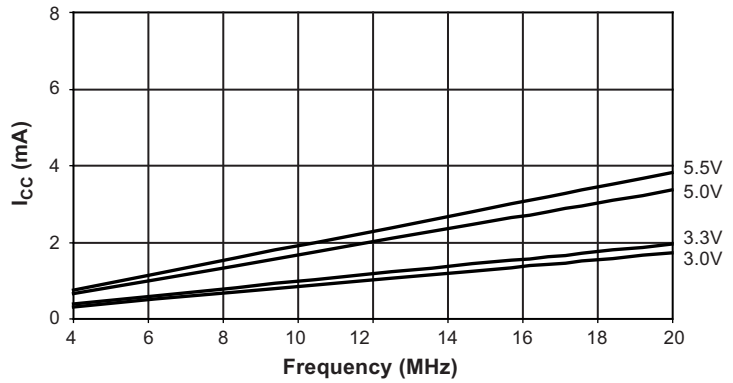


Figure 2-2. Idle Supply Current versus Frequency (1MHz to 20MHz)



2.2 Power-Down Supply Current

Figure 2-3. Power-down Supply Current versus V_{CC} (Watchdog Timer Disabled)

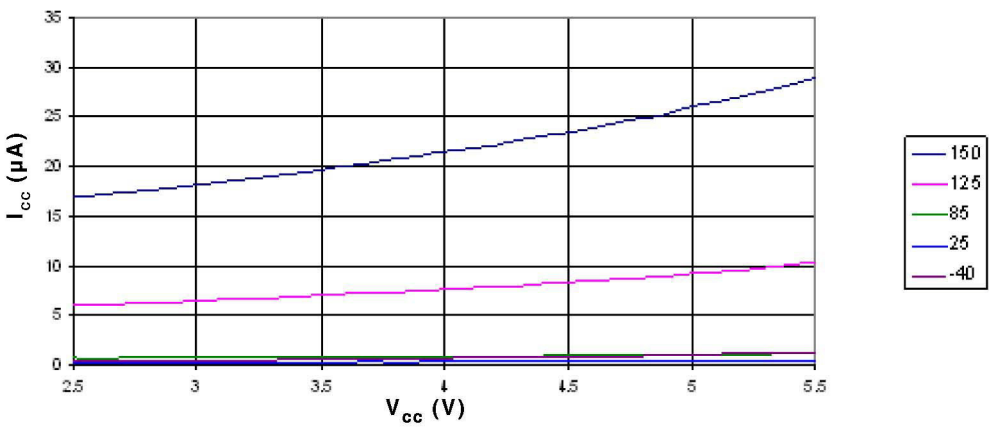
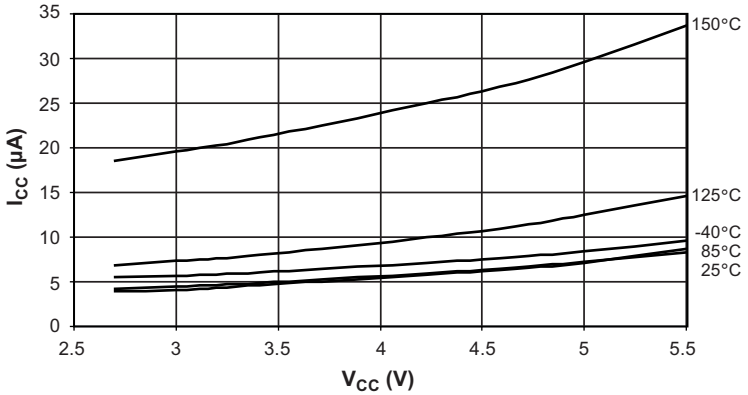


Figure 2-4. Power-down Supply Current versus V_{CC} (Watchdog Timer Enabled)



2.3 Pin Pull-up

Figure 2-5. I/O Pin Pull-up Resistor Current versus Input Voltage (V_{CC} = 5V)

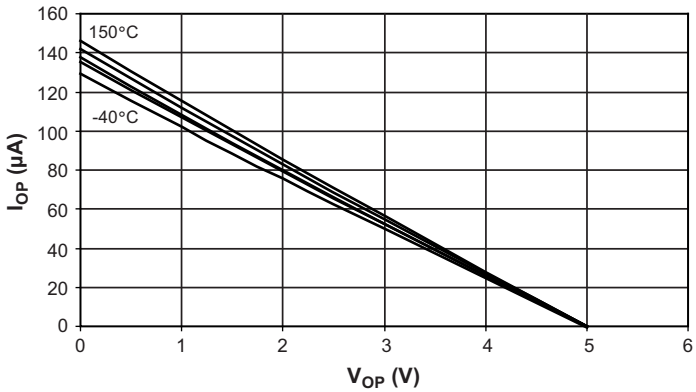


Figure 2-6. Output Low Voltage versus Output Low Current (V_{CC} = 5V)

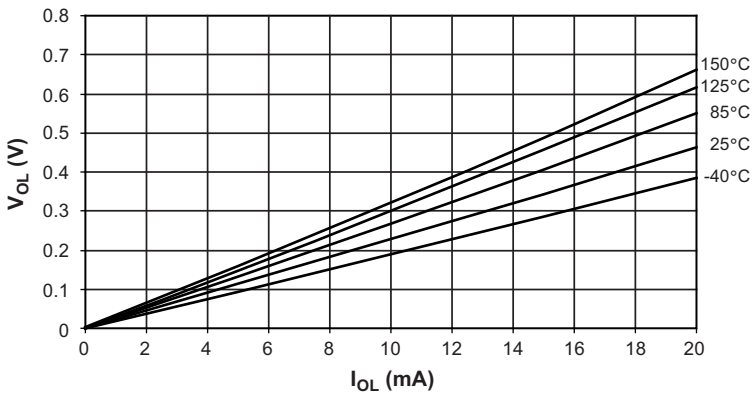


Figure 2-7. Output Low Voltage versus Output Low Current (V_{CC} = 3V)

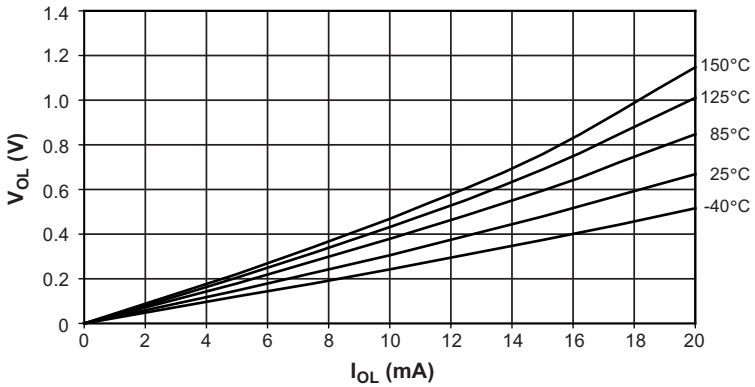


Figure 2-8. Output High Voltage versus Output High Current (V_{CC} = 5V)

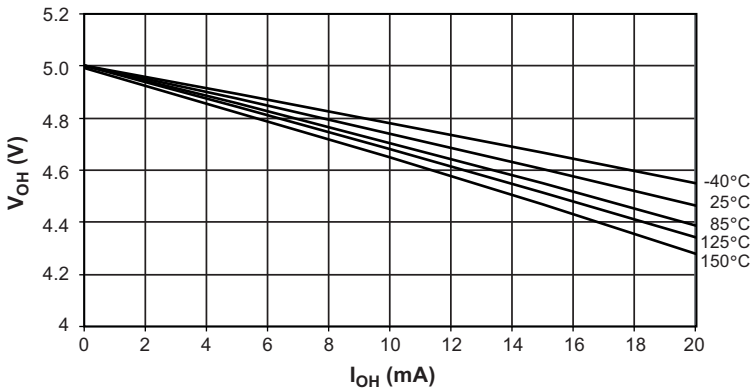


Figure 2-9. Output High Voltage versus Output High Current (V_{CC} = 3V)

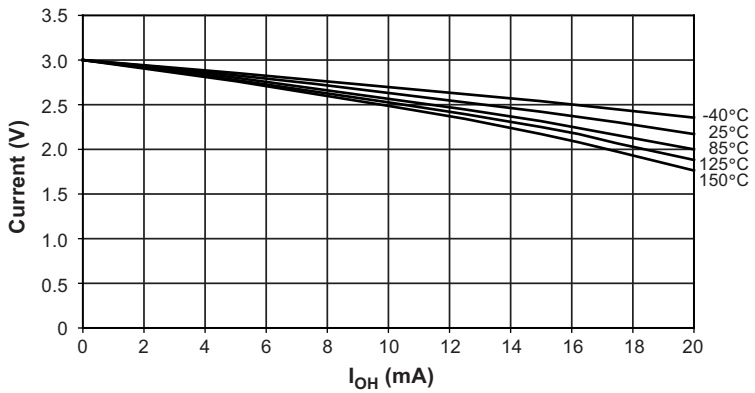
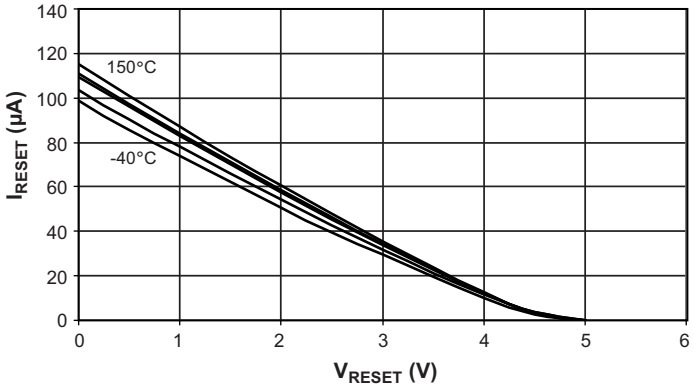


Figure 2-10. Reset Pull-up Resistor Current versus Reset Pin Voltage (V_{CC} = 5V)



2.4 Pin Thresholds and Hysteresis

Figure 2-11. I/O Pin Input Threshold versus V_{CC} (VIH, I/O Pin Read as '1')

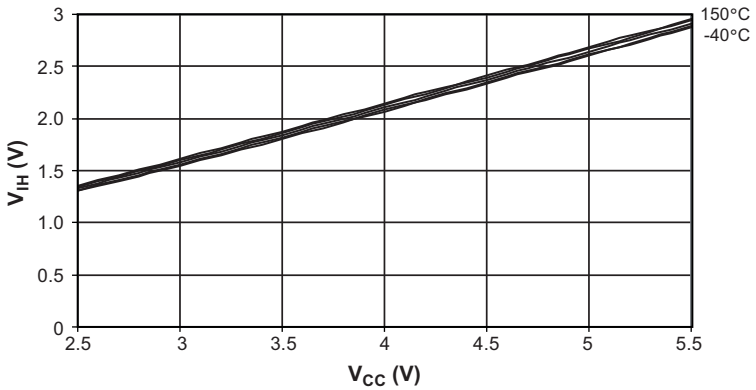


Figure 2-12. I/O Pin Input Threshold versus V_{CC} (VIL, I/O Pin Read as '0')

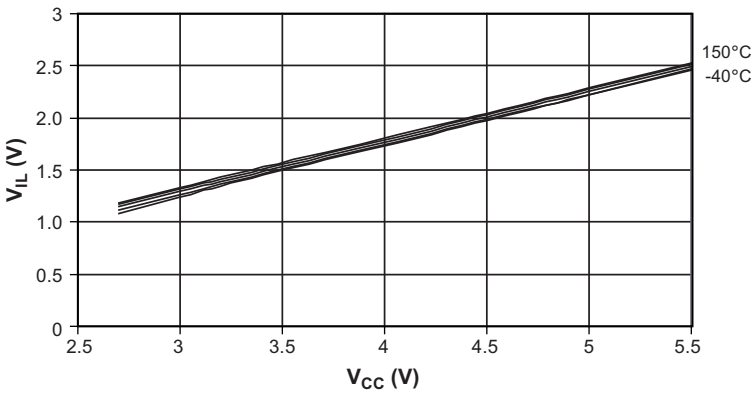


Figure 2-13. Reset Input Threshold Voltage versus V_{CC} (VIH, Reset Pin Read as '1')

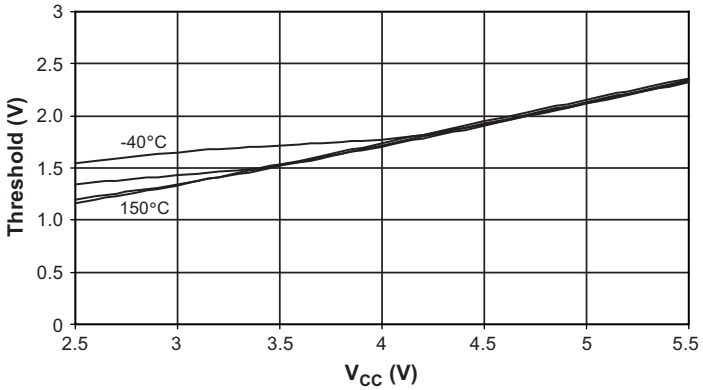
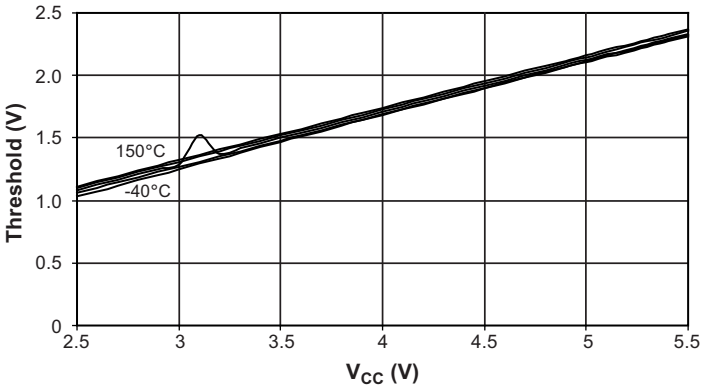


Figure 2-14. Reset Input Threshold Voltage versus V_{CC} (VIL, Reset Pin Read as '0')



2.5 Internal Oscillator Speed

Figure 2-15. Watchdog Oscillator Frequency versus V_{CC}

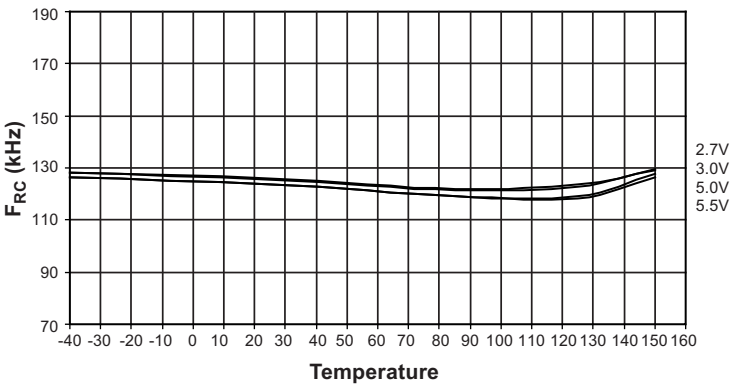


Figure 2-16. Calibrated 8MHz RC Oscillator Frequency versus Temperature

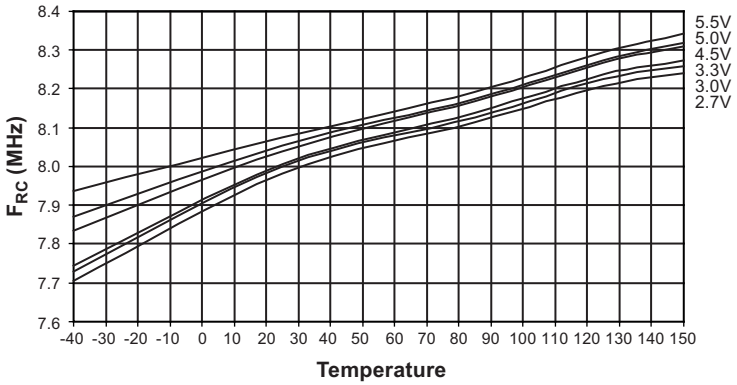


Figure 2-17. Calibrated 8MHz RC Oscillator Frequency versus V_{CC}

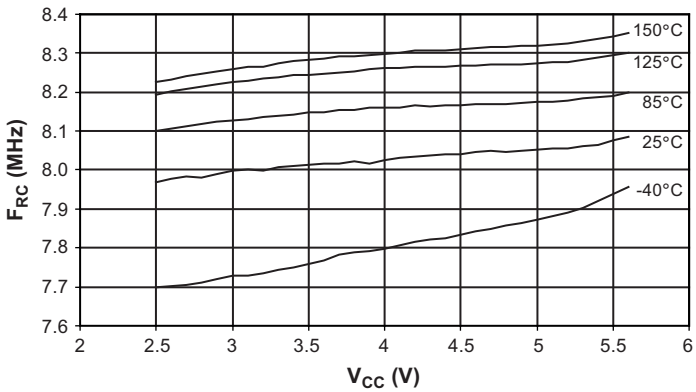
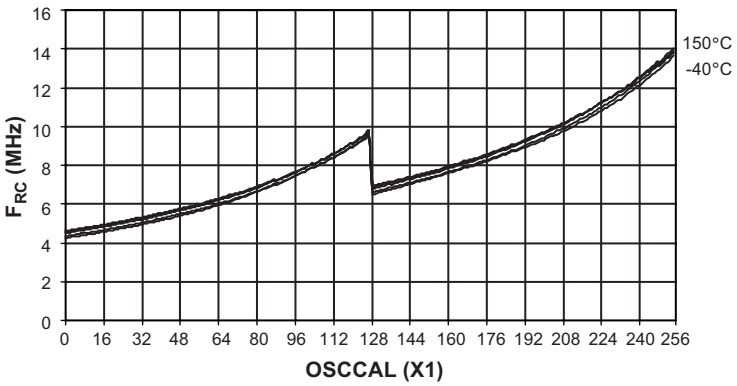


Figure 2-18. Calibrated 8MHz RC Oscillator Frequency versus OSCCAL Value



2.6 BOD Thresholds and Analog Comparator Offset

Figure 2-19. BOD Threshold versus Temperature (BODLEVEL is 4.0V)

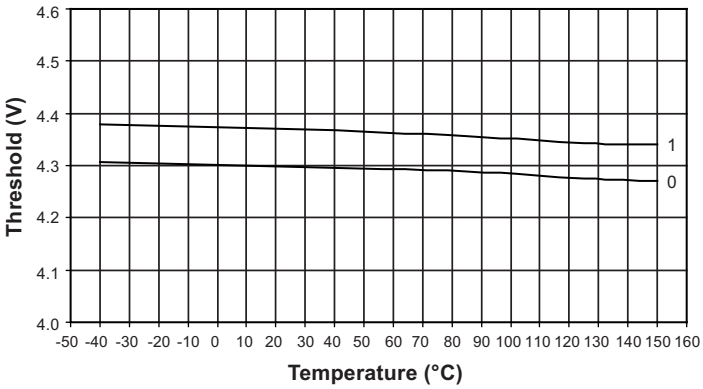


Figure 2-20. BOD Threshold versus Temperature (BODLEVEL is 2.7V)

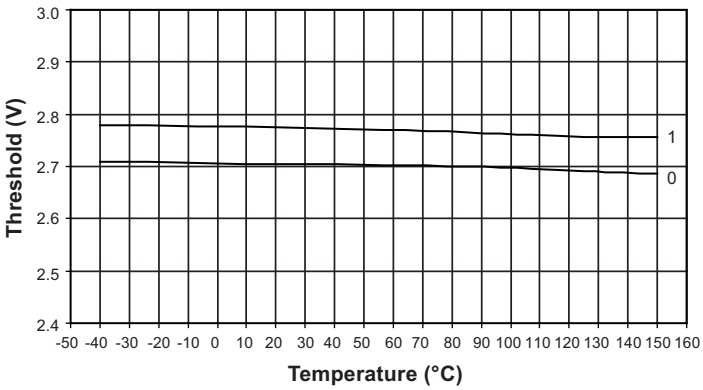
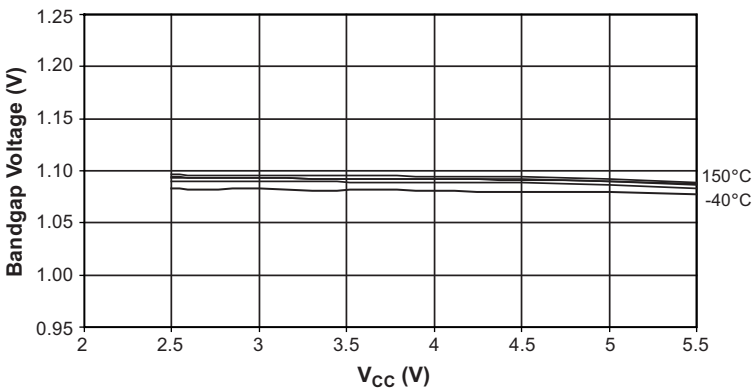


Figure 2-21. Bandgap Voltage versus V_{CC}



2.7 Peripheral Units

Figure 2-22. Analog to Digital Converter GAIN versus V_{CC}

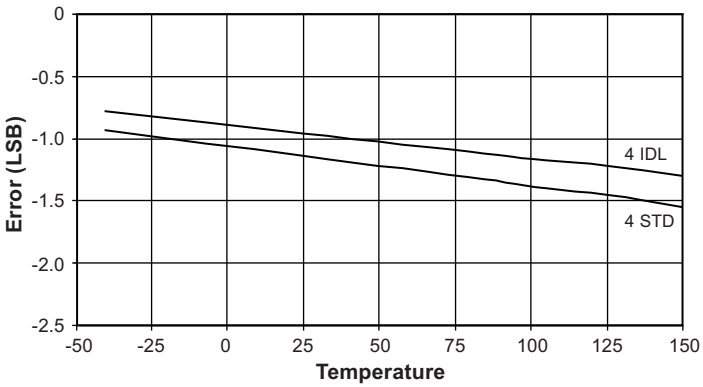


Figure 2-23. Analog to Digital Converter OFFSET versus V_{CC}

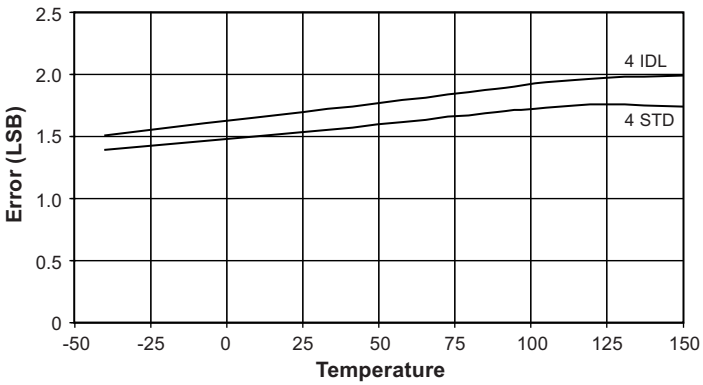


Figure 2-24. Analog to Digital Converter DNL versus V_{CC}

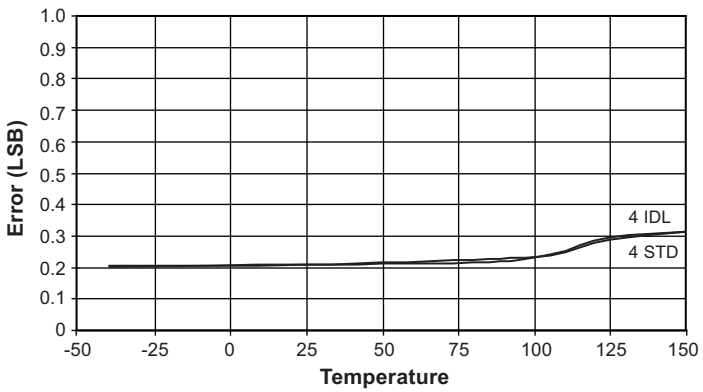
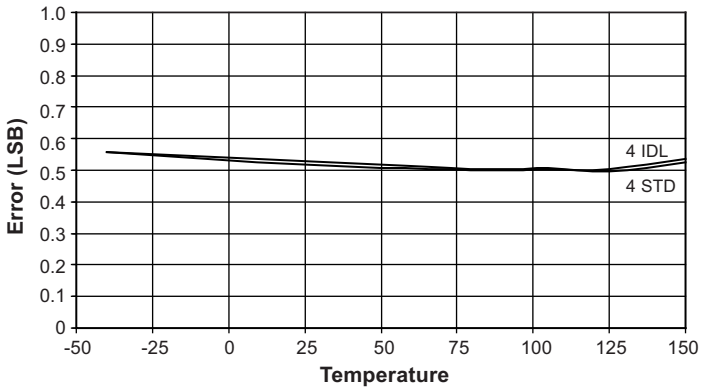


Figure 2-25. Analog to Digital Converter INL versus V_{CC}



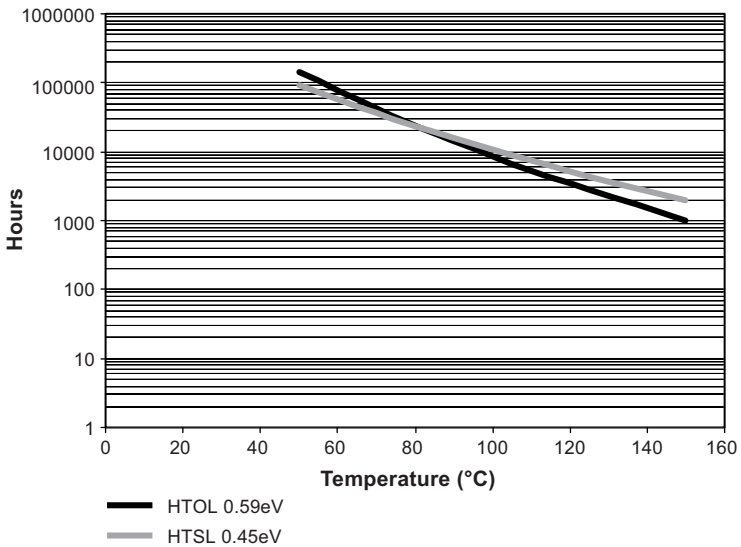
2.8 Grade 0 Qualification

The ATmega88/168 has been developed and manufactured according to the most stringent quality assurance requirements of ISO-TS-16949 and verified during product qualification as per AEC-Q100 grade 0.

AEC-Q100 qualification relies on temperature accelerated stress testing. High temperature field usage however may result in less significant stress test acceleration. In order to prevent the risk that ATmega88/168 lifetime would not satisfy the application end-of-life reliability requirements, Atmel® has extended the testing, whenever applicable (High Temperature Operating Life Test, High Temperature Storage Life, Data Retention, Thermal Cycles), far beyond the AEC-Q100 requirements. Thereby, Atmel verified the ATmega88/168 has a long safe lifetime period after the grade 0 qualification acceptance limits.

The valid domain calculation depends on the activation energy of the potential failure mechanism that is considered. Examples are given in Figure 2-26. Therefore any temperature mission profile which could exceed the AEC-Q100 equivalence domain shall be submitted to Atmel for a thorough reliability analysis.

Figure 2-26. AEC-Q100 Lifetime Equivalence



3. Ordering Information

Table 3-1. ATmega88/168

Speed (MHz)	Power Supply	Ordering Code	Package[1]	Operation Range
16[2]	2.7V to 5.5V	ATmega88-15MT2	PN	Extended (–40°C to +150°C)
16[2]	2.7V to 5.5V	ATmega88-15AD	MA	Extended (–40°C to +150°C)
16[2]	2.7V to 5.5V	ATmega168-15MD	PN	Extended (–40°C to +150°C)
16[2]	2.7V to 5.5V	ATmega168-15AD	MA	Extended (–40°C to +150°C)

Notes: 1. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also halide free and fully green.

2. For speed versus V_{cc}, see complete datasheet.

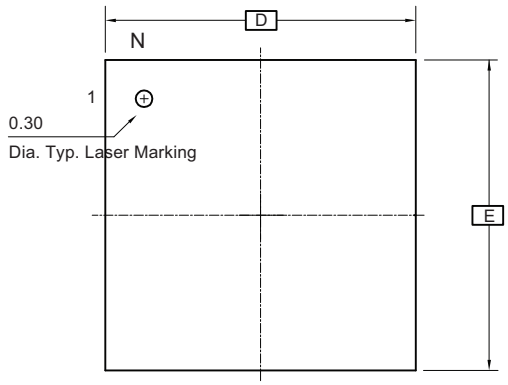
4. Package Information

Table 4-1. Package Types

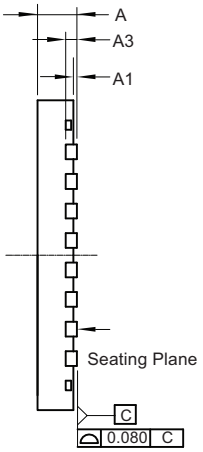
Package Type	
PN	32-pad, 5 × 5 ×1.0mm body, lead pitch 0.50mm, quad flat no-lead/micro lead frame package (QFN/MLF): E2/D2 3.1 ±0.1mm
MA	32 - Lead, 7mm × 7mm body size, 1.0mm body thickness 0.8mm lead pitch, thin profile plastic quad flat package (TQFP)

Figure 4-1. PN

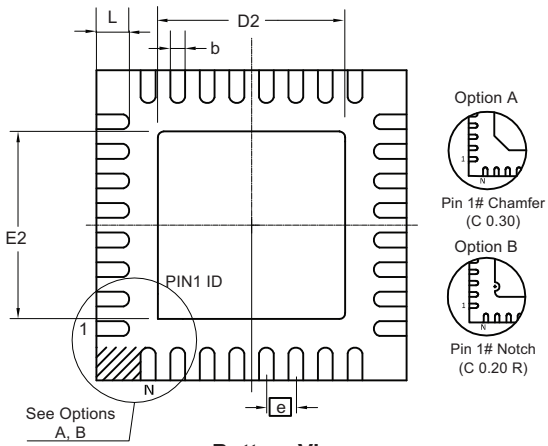
Drawings not scaled



Top View



Side View



Bottom View

COMMON DIMENSIONS (Unit of Measure = mm)				
Symbol	**MIN**	**NOM**	**MAX**	**NOTE**
A	0.80	0.85	0.90	
A1	0.00	----	0.05	
A3		0.20 REF		
D/E		5.00 BSC		
D2/E2	3.00	3.10	3.20	
L	0.30	0.40	0.50	
b	0.18	0.25	0.30	2
e		0.50 BSC		
n		32		

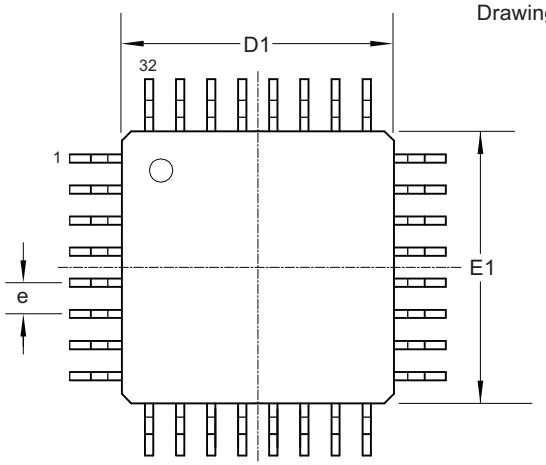
Notes: 1. This drawing is for general information only. Refer to JEDEC Drawing MO-220, Variation VHHD-2, for proper dimensions, tolerances, datums, etc.
2. Dimensions b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has the optical radius on the other end of the terminal, the dimensions should not be measured in that radius area.

01/31/12

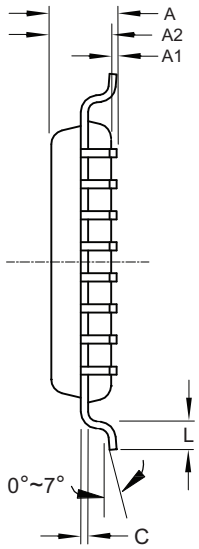
Atmel **Package Drawing Contact:** packagedrawings@atmel.com	TITLE	GPC	DRAWING NO.	REV.
	PN, 32 Leads - 0.50mm Pitch, 5x5mm Very Thin Quad Flat no Lead Package (VQFN) Sawn	ZMF	PN	I

Figure 4-2. MA

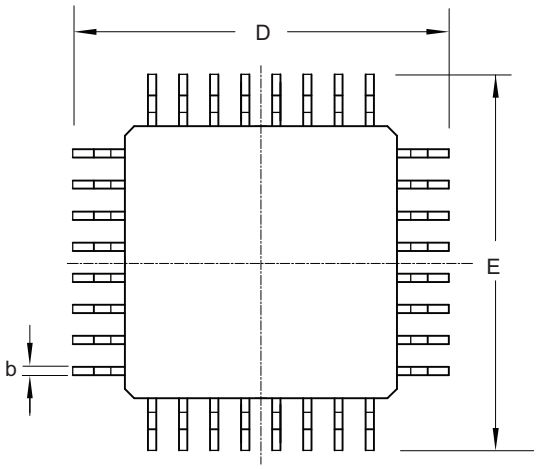
Drawings not scaled



Top View



Side View



Bottom View

COMMON DIMENSIONS (Unit of Measure = mm)				
Symbol	**MIN**	**NOM**	**MAX**	**NOTE**
A	----	----	1.20	
A1	0.05	----	0.15	
A2	0.95	1.00	1.05	
D/E	8.75	9.00	9.25	
D1/E1	6.90	7.00	7.10	2
C	0.09	----	0.20	
L	0.45	----	0.75	
b	0.30	----	0.45	
e	0.80 TYP.			
n	32			

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MS-026, Variation ABA.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10mm maximum.

02/29/12

Atmel **Package Drawing Contact:** packagedrawings@atmel.com	TITLE	GPC	DRAWING NO.	REV.
	MA, 32 Lds - 0.80mm Pitch, 7x7x1.00mm Body size Thin Profile Plastic Quad Flat Package (TQFP)	AUT	MA	C

5. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
7607J-AVR-07/14	• Put datasheet in the latest template
7607I-AVR-03/12	• Section 4 “Package Information” on pages 15 to 16 changed
7607H-AVR-02/10	• Table 4-1 “Package Types” on page 15 changed
7607G-AVR-07/09	• Package MA updated
7607F-AVR-01/08	• Added memory endurance. See Section 1.3 “Memory Endurance” on page 4
7607E-AVR-11/07	• Added ATMega168 product offering • Added MA package offering
7607D-AVR-03/07	• Updated electrical characteristics • Removed Grade0 qualification section • Updated product part number in ordering information
7607C-AVR-09/06	• Ordering and package information updated
7607B-AVR-08/06	• Added typical characteristics
7607A-AVR-01/06	• Document Creation

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