

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4029B

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Synchronous up/down counter,
binary/decade counter

Product specification
File under Integrated Circuits, IC04

January 1995

Synchronous up/down counter,
binary/decade counter

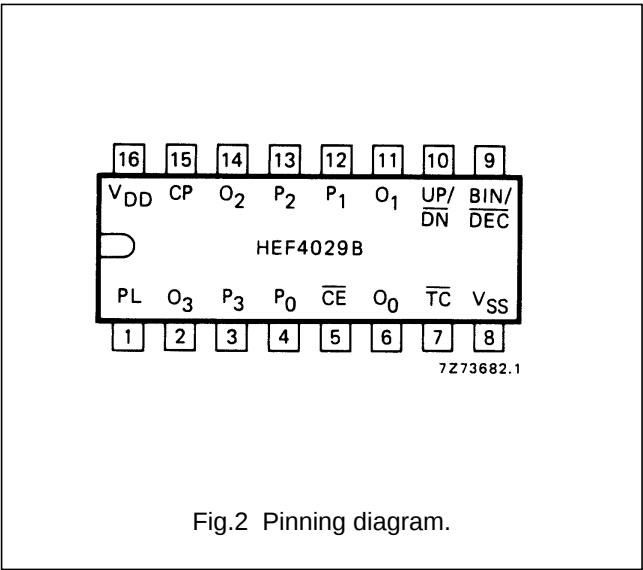
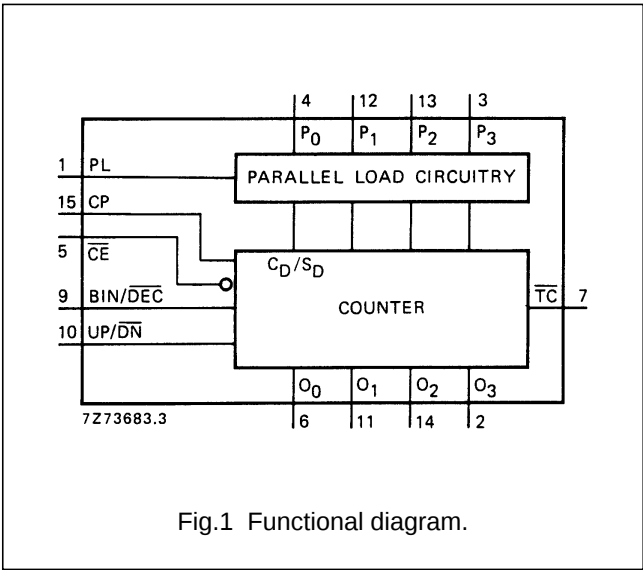
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DESCRIPTION

The HEF4029B is a synchronous edge-triggered up/down 4-bit binary/BCD decade counter with a clock input (CP), an active LOW count enable input ($\overline{\text{CE}}$), an up/down control input ($\text{UP}/\overline{\text{DN}}$), a binary/decade control input ($\text{BIN}/\overline{\text{DEC}}$), an overriding asynchronous active HIGH parallel load input (PL), four parallel data inputs (P_0 to P_3), four parallel buffered outputs (O_0 to O_3) and an active LOW terminal count output ($\overline{\text{TC}}$).

Information on P_0 to P_3 is asynchronously loaded into the counter while PL is HIGH, independent of CP.

The counter is advanced one count on the LOW to HIGH transition of CP when $\overline{\text{CE}}$ and PL are LOW. The $\overline{\text{TC}}$ signal is normally HIGH and goes LOW when the counter reaches its maximum count in the UP mode, or the minimum count in the DOWN mode provided $\overline{\text{CE}}$ is LOW.



- HEF4029BP(N): 16-lead DIL; plastic (SOT38-1)
- HEF4029BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
- HEF4029BT(D): 16-lead SO; plastic (SOT109-1)
- (): Package Designator North America

PINNING

- PL parallel load input
- P_0 to P_3 parallel data inputs
- $\text{BIN}/\overline{\text{DEC}}$ binary/decade control input
- $\text{UP}/\overline{\text{DN}}$ up/down control input
- $\overline{\text{CE}}$ count enable input (active LOW)
- CP clock input (LOW to HIGH, edge triggered)
- O_0 to O_3 buffered parallel outputs
- $\overline{\text{TC}}$ terminal count output (active LOW)

FAMILY DATA, I_{DD} LIMITS category MSI

See Family Specifications

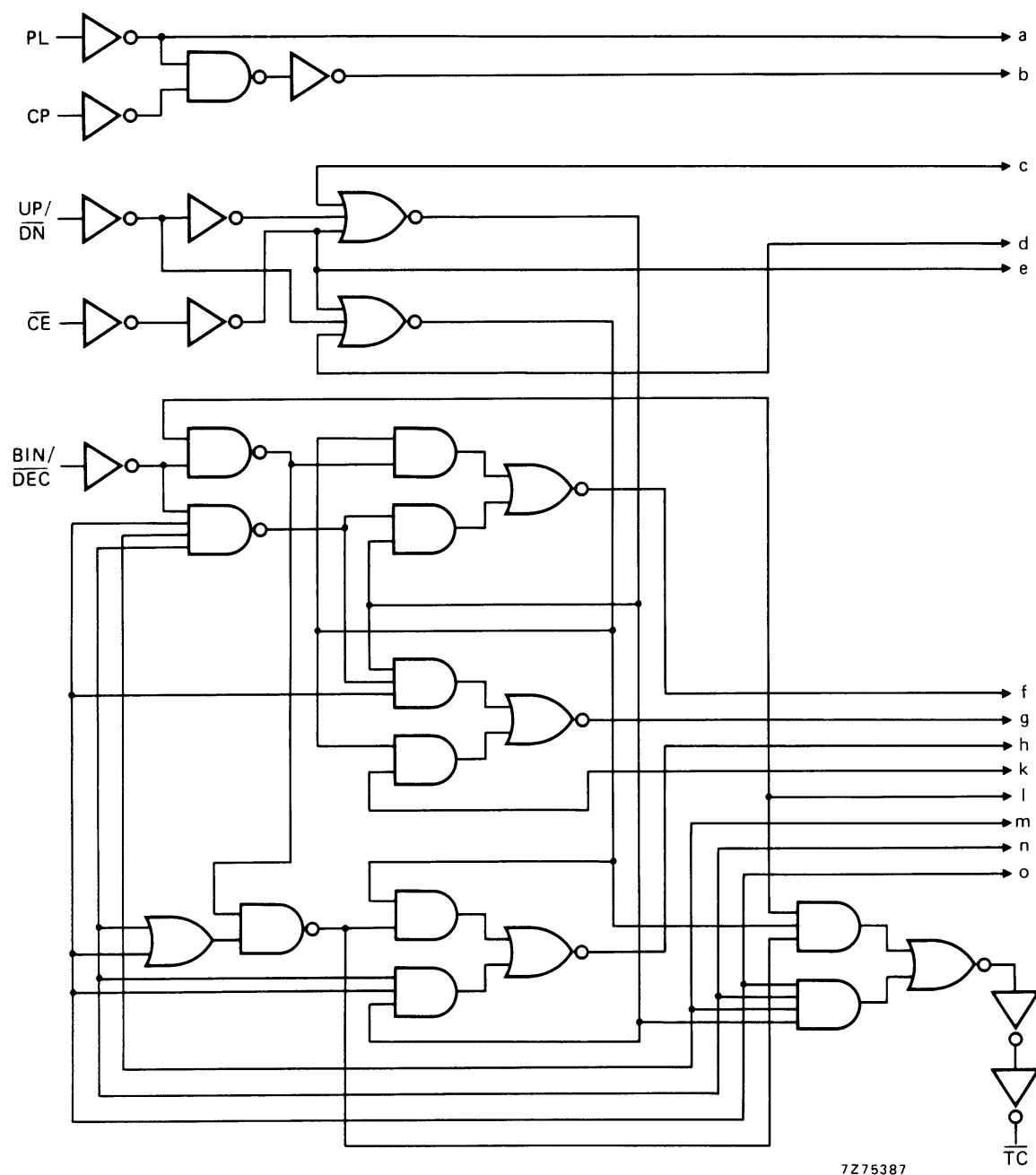
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Fig.3 Logic diagram (continued in Fig.4).

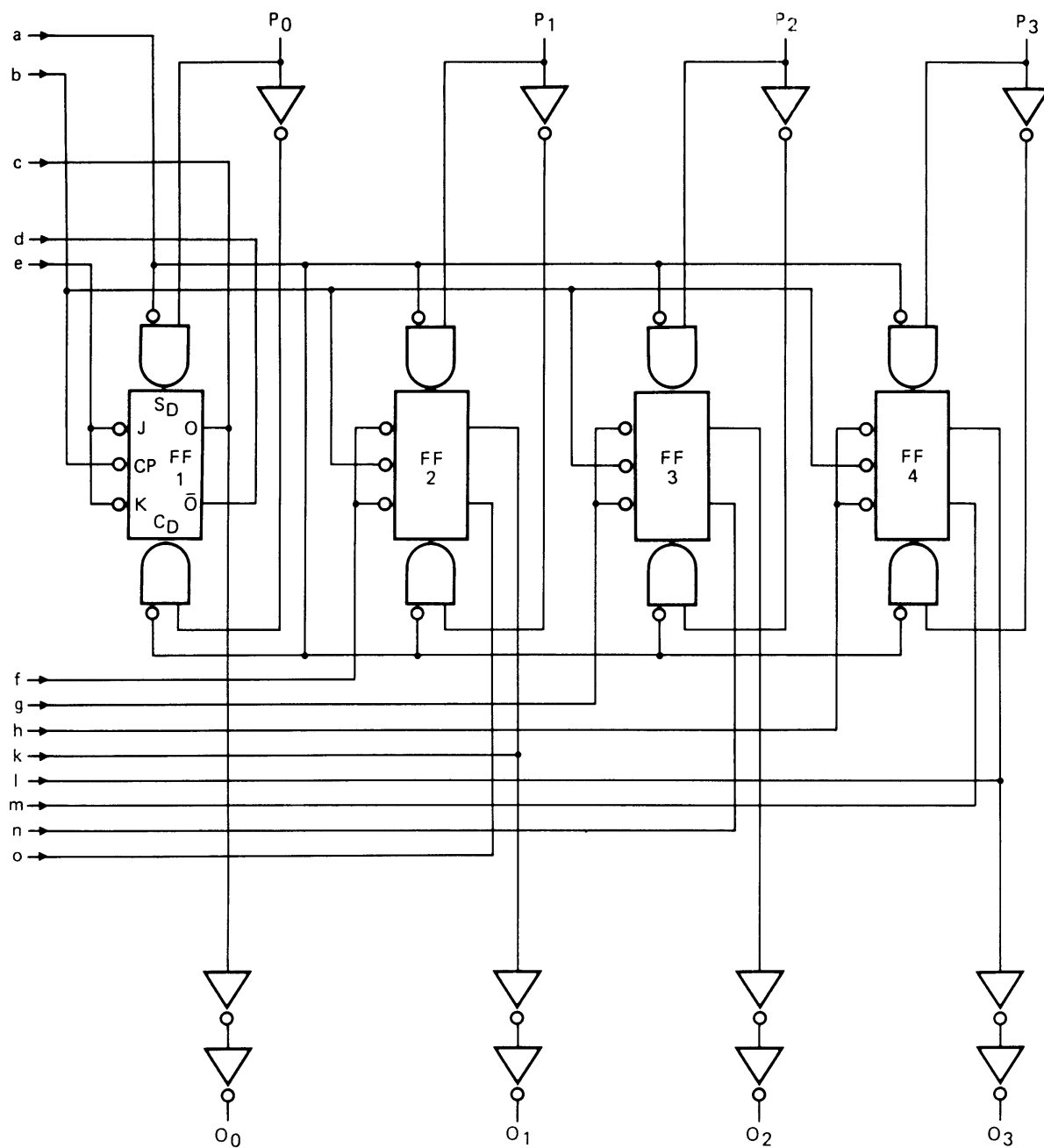
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Fig.4 Logic diagram (continued from Fig.3).

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FUNCTION TABLE

PL	BIN/DEC	UP/DN	CE	CP	MODE
H	X	X	X	X	parallel load ($P_n \rightarrow O_n$)
L	X	X	H	X	no change
L	L	L	L		count-down, decade
L	L	H	L		count-up, decade
L	H	L	L		count-down, binary
L	H	H	L		count-up, binary

Notes

1. H = HIGH state (the more positive voltage)
- L = LOW state (the less positive voltage)
- X = state is immaterial
-  = positive-going clock pulse edge

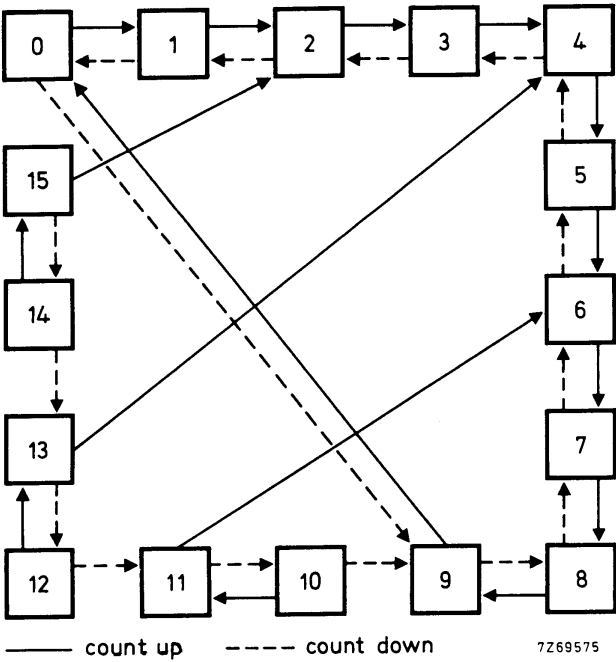


Fig.5 State diagram; BIN/DEC = LOW.

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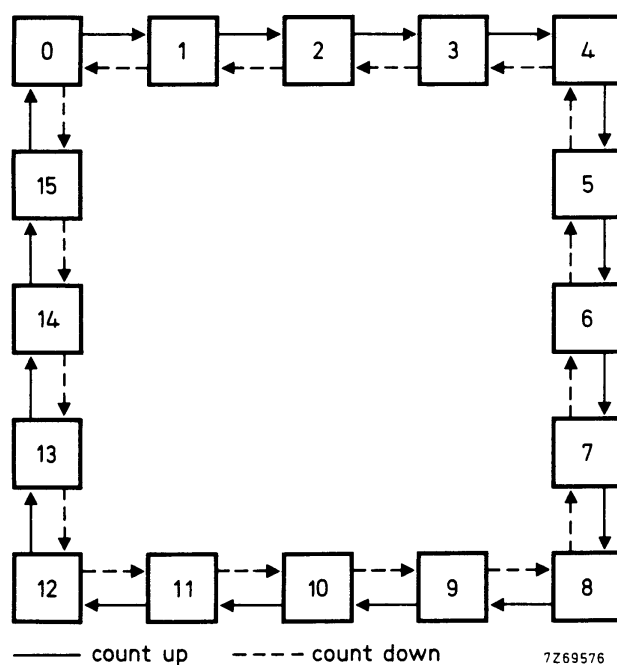


Fig.6 State diagram; $\overline{\text{BIN/DEC}} = \text{HIGH}$.

Logic equation for terminal count:

$$\text{TC} = \overline{\text{CE}} (\overline{\text{BIN/DEC}} \cdot \text{UP}/\overline{\text{DN}} \cdot \text{O}_0 \cdot \text{O}_1 \cdot \text{O}_2 \cdot \text{O}_3 + \overline{\text{BIN/DEC}} \cdot \text{UP}/\overline{\text{DN}} \cdot \overline{\text{O}}_0 \cdot \overline{\text{O}}_1 \cdot \overline{\text{O}}_2 \cdot \overline{\text{O}}_3 + \\ \overline{\text{BIN/DEC}} \cdot \text{UP}/\overline{\text{DN}} \cdot \text{O}_0 \cdot \text{O}_3 + \overline{\text{BIN/DEC}} \cdot \text{UP}/\overline{\text{DN}} \cdot \overline{\text{O}}_0 \cdot \overline{\text{O}}_1 \cdot \overline{\text{O}}_2 \cdot \overline{\text{O}}_3)$$

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AC CHARACTERISTICS

$V_{SS} = 0$ V; $T_{amb} = 25$ °C; input transition times ≤ 20 ns

	V_{DD} V	TYPICAL FORMULA FOR P (μ W)	
Dynamic power dissipation per package (P)	5 10 15	$1000 f_i + \sum(f_o C_L) \times V_{DD}^2$ $4500 f_i + \sum(f_o C_L) \times V_{DD}^2$ $11\,500 f_i + \sum(f_o C_L) \times V_{DD}^2$	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\sum(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)

AC CHARACTERISTICS

$V_{SS} = 0$ V; $T_{amb} = 25$ °C; $C_L = 50$ pF; input transition times ≤ 20 ns

	V _{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA	
Propagation delays							
CP → O _n HIGH to LOW	5 10 15	t _{PHL}		145 55 40	290 110 75	ns ns ns	118 ns + (0,55 ns/pF) C _L 44 ns + (0,23 ns/pF) C _L 32 ns + (0,16 ns/pF) C _L
LOW to HIGH	5 10 15	t _{PLH}		160 60 40	315 120 80	ns ns ns	133 ns + (0,55 ns/pF) C _L 49 ns + (0,23 ns/pF) C _L 32 ns + (0,16 ns/pF) C _L
CP → $\overline{TC}$ HIGH to LOW	5 10 15	t _{PHL}		280 105 70	560 205 140	ns ns ns	253 ns + (0,55 ns/pF) C _L 94 ns + (0,23 ns/pF) C _L 62 ns + (0,16 ns/pF) C _L
LOW to HIGH	5 10 15	t _{PLH}		195 75 55	385 150 105	ns ns ns	168 ns + (0,55 ns/pF) C _L 64 ns + (0,23 ns/pF) C _L 47 ns + (0,16 ns/pF) C _L
PL → O _n HIGH to LOW	5 10 15	t _{PHL}		120 50 35	240 100 70	ns ns ns	93 ns + (0,55 ns/pF) C _L 39 ns + (0,23 ns/pF) C _L 27 ns + (0,16 ns/pF) C _L
LOW to HIGH	5 10 15	t _{PLH}		170 65 45	335 130 90	ns ns ns	143 ns + (0,55 ns/pF) C _L 54 ns + (0,23 ns/pF) C _L 37 ns + (0,16 ns/pF) C _L
$\overline{CE} \rightarrow \overline{TC}$ HIGH to LOW	5 10 15	t _{PHL}		180 70 50	360 140 100	ns ns ns	153 ns + (0,55 ns/pF) C _L 59 ns + (0,23 ns/pF) C _L 42 ns + (0,16 ns/pF) C _L
LOW to HIGH	5 10 15	t _{PLH}		170 65 50	335 135 100	ns ns ns	143 ns + (0,55 ns/pF) C _L 54 ns + (0,23 ns/pF) C _L 42 ns + (0,16 ns/pF) C _L

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	V _{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA
Output transition times HIGH to LOW	5	t _{THL}		60	120 ns	10 ns + (1,0 ns/pF) C _L
	10			30	60 ns	9 ns + (0,42 ns/pF) C _L
	15			20	40 ns	6 ns + (0,28 ns/pF) C _L
LOW to HIGH	5	t _{TLH}		60	120 ns	10 ns + (1,0 ns/pF) C _L
	10			30	60 ns	9 ns + (0,42 ns/pF) C _L
	15			20	40 ns	6 ns + (0,28 ns/pF) C _L

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AC CHARACTERISTICS

$V_{SS} = 0$ V; $T_{amb} = 25$ °C; $C_L = 50$ pF; input transition times ≤ 20 ns

	V_{DD} V	SYMBOL	MIN	TYP	MAX	
Minimum clock pulse width; LOW	5	t_{WCPL}	110	55	ns	see also waveforms Figs 7 and 8
	10		35	20	ns	
	15		25	15	ns	
Minimum PL pulse width; HIGH	5	t_{WPLH}	160	80	ns	
	10		55	25	ns	
	15		35	15	ns	
Recovery time for PL	5	t_{RPL}	150	75	ns	
	10		50	25	ns	
	15		35	20	ns	
Set-up times $\overline{BIN}/\overline{DEC} \rightarrow CP$	5	t_{su}	270	135	ns	
	10		90	45	ns	
	15		60	30	ns	
	5	t_{su}	300	150	ns	
	10		105	55	ns	
	15		75	35	ns	
	5	t_{su}	240	120	ns	
	10		90	50	ns	
	15		70	40	ns	
$P_n \rightarrow PL$	5	t_{su}	70	35	ns	
	10		20	10	ns	
	15		10	5	ns	
Hold times $\overline{BIN}/\overline{DEC} \rightarrow CP$	5	t_{hold}	45	-90	ns	
	10		15	-30	ns	
	15		10	-20	ns	
	5	t_{hold}	15	-135	ns	
	10		0	-50	ns	
	15		-5	-35	ns	
	5	t_{hold}	30	-30	ns	
	10		10	-10	ns	
	15		5	-10	ns	
	5	t_{hold}	15	-20	ns	
	10		0	-10	ns	
	15		0	-5	ns	
Maximum clock pulse frequency	5	f_{max}	2	4	MHz	
	10		5	10	MHz	
	15		8	15	MHz	

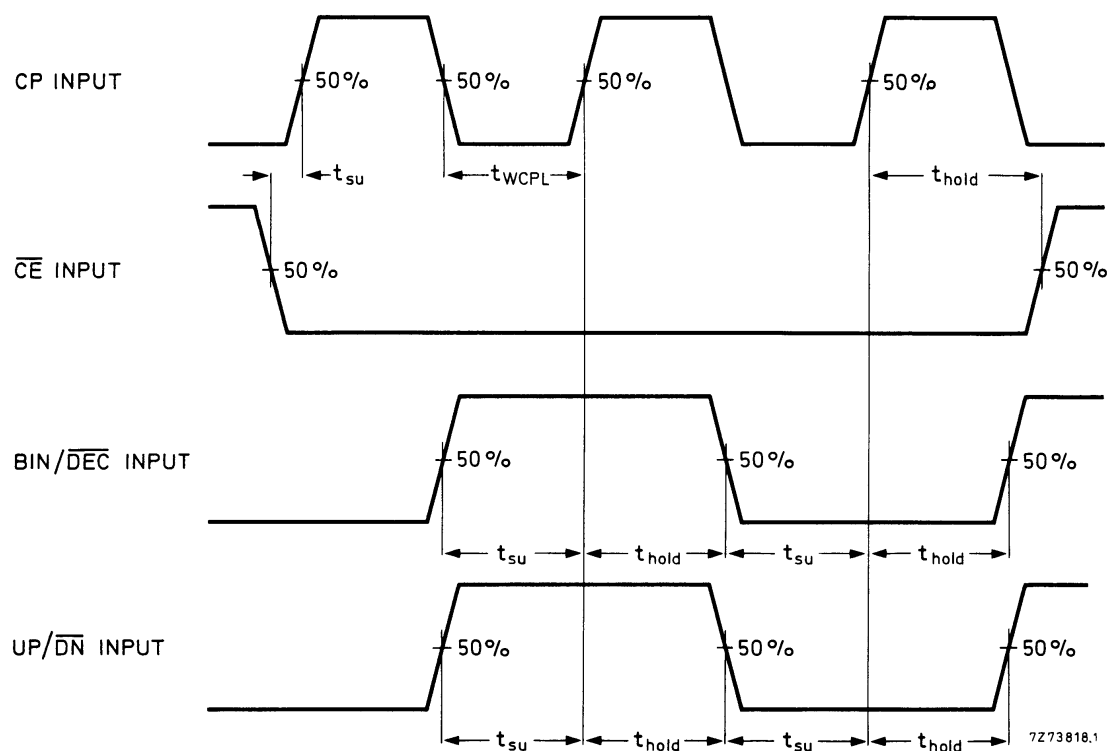
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Fig.7 Waveforms showing minimum pulse width for CP, set-up and hold times for $\overline{CE}$ to CP, BIN/ $\overline{DEC}$ to CP and UP/ $\overline{DN}$ to CP. Set-up and hold times are shown as positive values but may be specified as negative values.

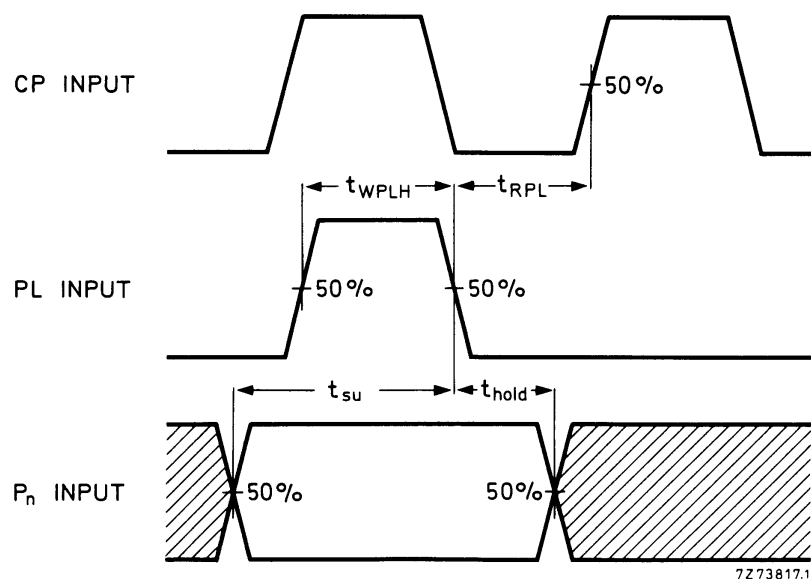


Fig.8 Waveforms showing minimum pulse width for PL, recovery time for PL, and set-up and hold times for P_n to PL. Set-up and hold times are shown as positive values but may be specified as negative values.

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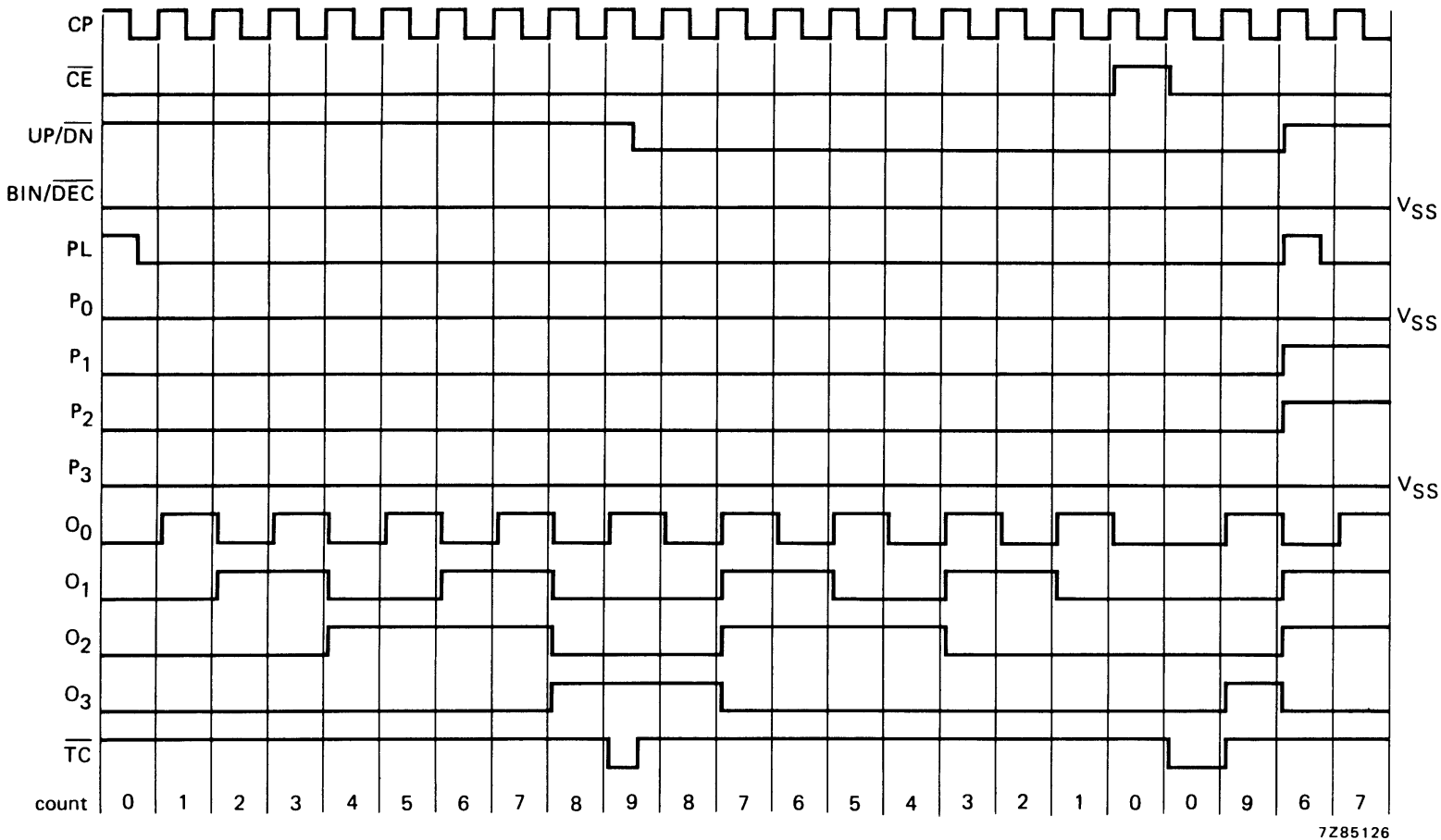


Fig.9 Timing diagram; decade mode; $P_0 = \text{LOW}$; $P_3 = \text{LOW}$; $\text{BIN}/\overline{\text{DEC}} = \text{LOW}$.

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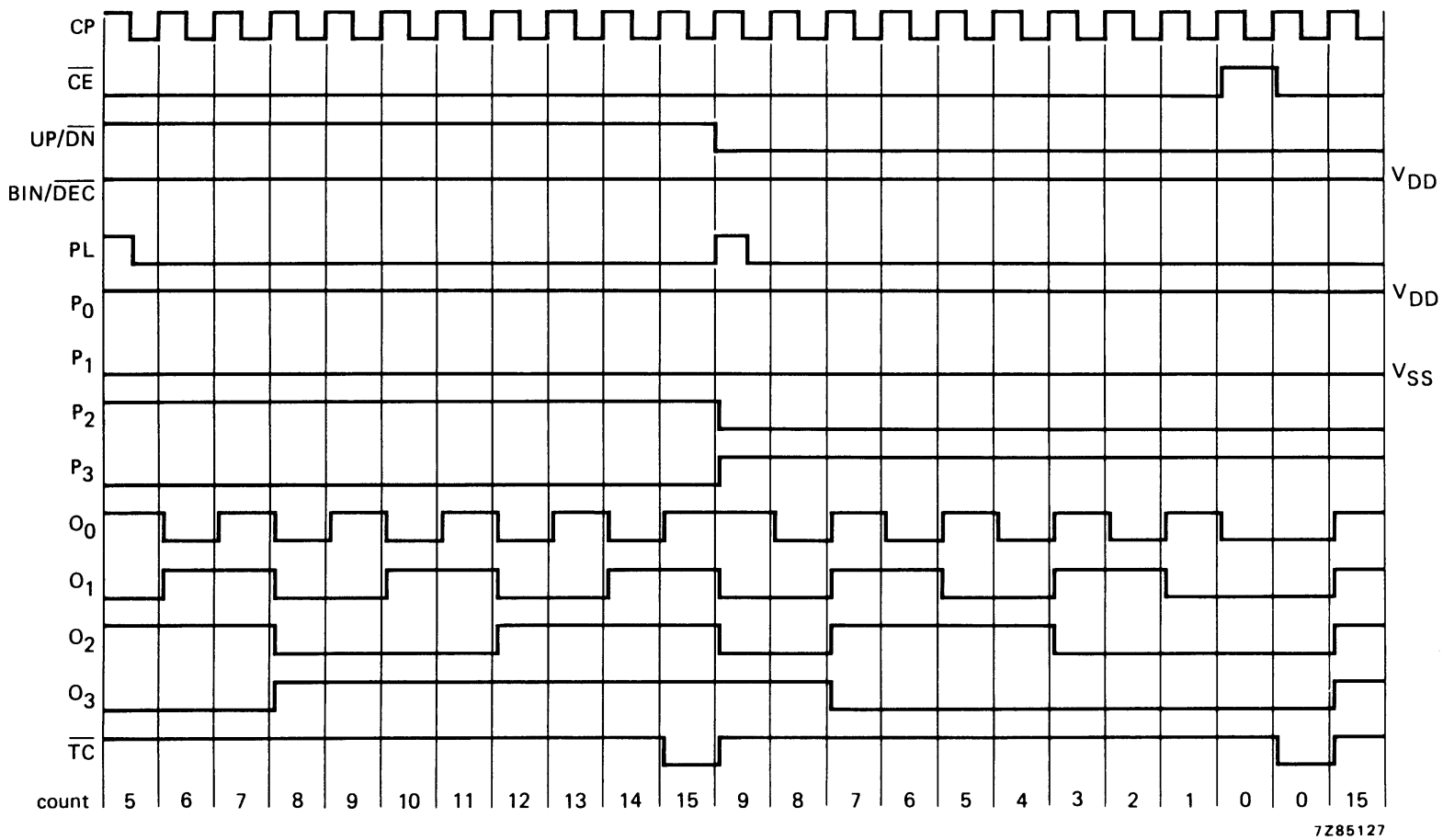


Fig.10 Timing diagram; binary mode; P₀ = HIGH; P₁ = LOW; BIN/DEC = HIGH.

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APPLICATION INFORMATION

Some examples of applications for the HEF4029B are:

- Programmable binary and decade counting/frequency synthesizers - BCD output.
- Analogue-to-digital and digital-to-analogue conversion.
- Up/down binary counting.
- Magnitude and sign generation.
- Up/down decade counting.
- Difference counting.

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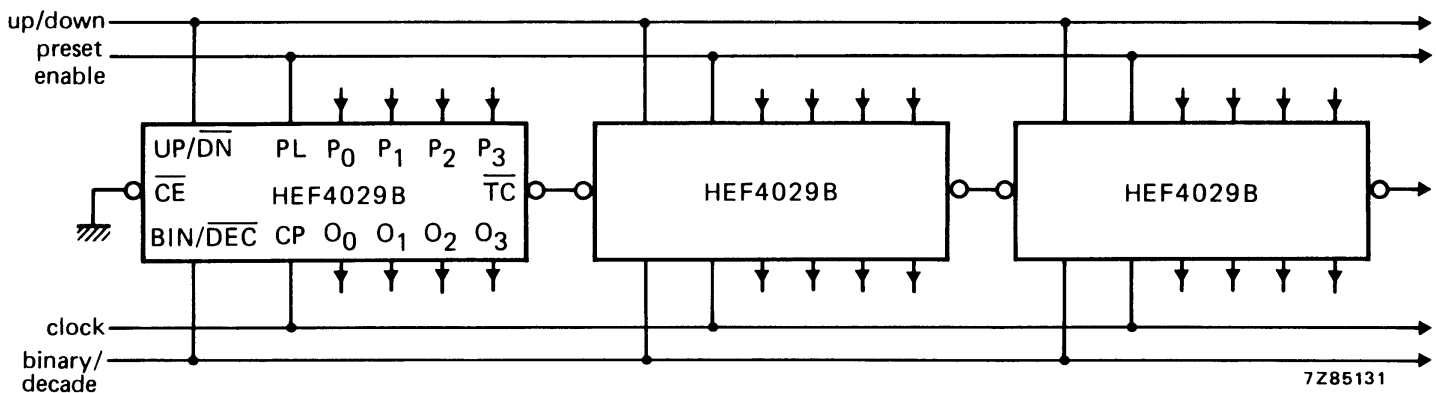
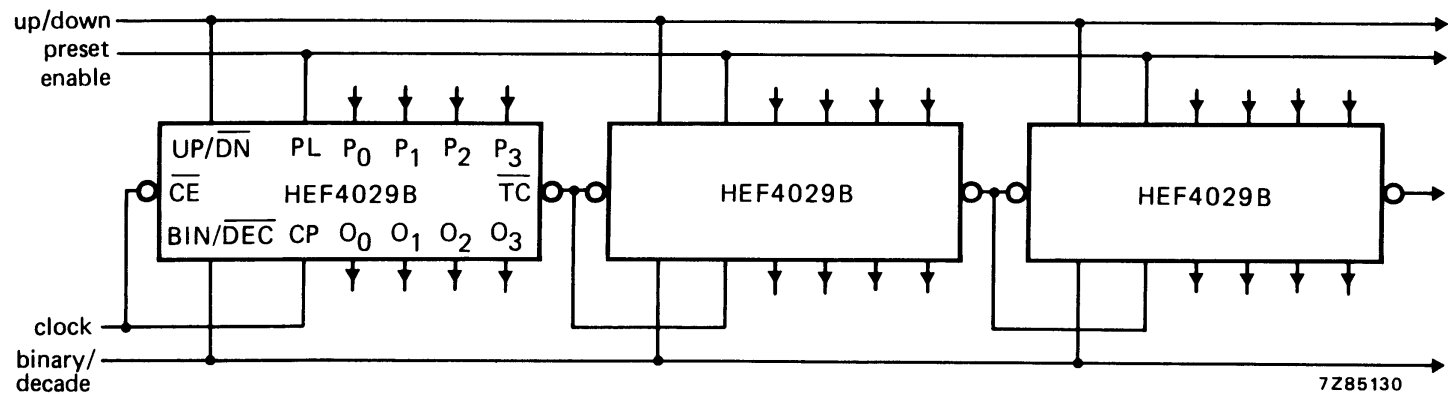


Fig.11 Example of parallel clocking when cascading HEF4029B ICs.



Note

$\overline{TC}$ lines at all stages after the first may have a negative-going glitch pulse resulting from differential delays of different HEF4029B ICs. These negative-going glitches do not affect proper HEF4029B operation; however if the $\overline{TC}$ signals are used to trigger other edge-sensitive logic devices, such as flip-flops or counters, the $\overline{TC}$ signals should be gated with the clock signal using a 2-input OR gate such as HEF4071B.

Fig.12 Example of ripple clocking when cascading HEF4029B ICs. Ripple clocking mode: the up/down control can be changed at any count; the only restriction on changing the up/down control is that the clock input to the first counting stage must be HIGH.