

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4020B

MSI

14-stage binary counter

Product specification
File under Integrated Circuits, IC04

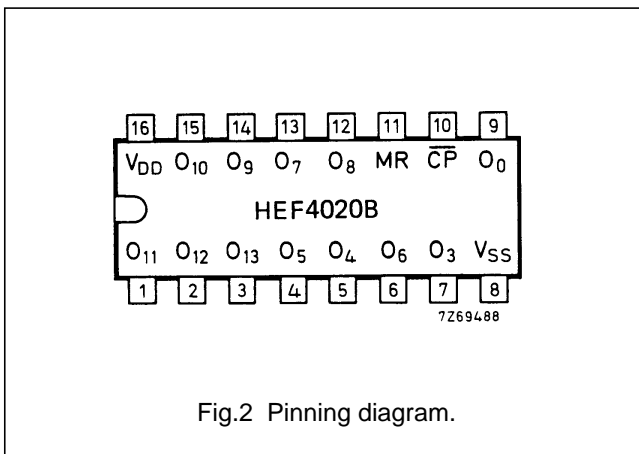
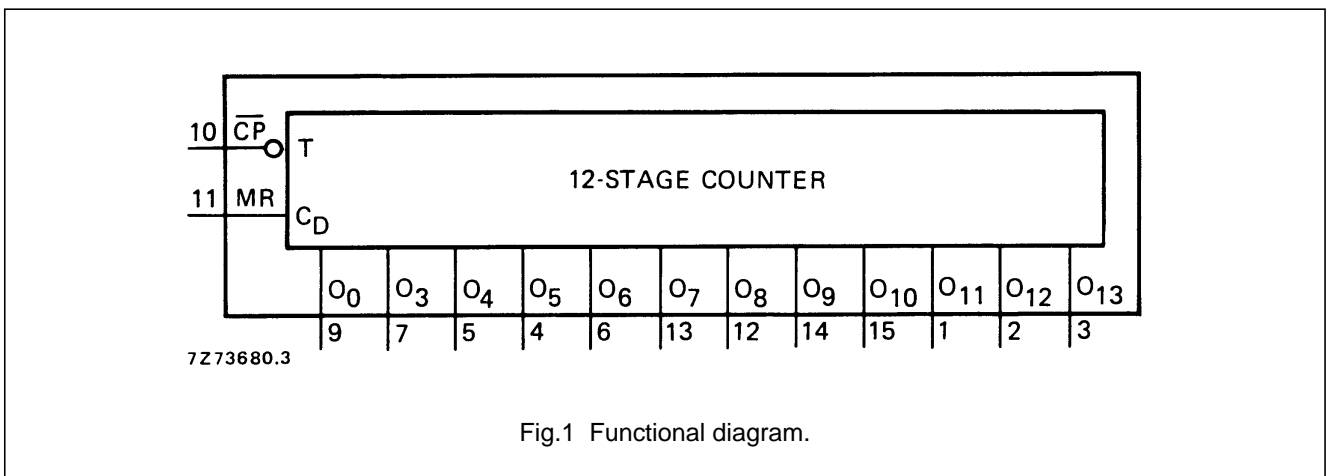
January 1995

14-stage binary counter

HEF4020B MSI

DESCRIPTION

The HEF4020B is a 14-stage binary ripple counter with a clock input (\overline{CP}), an overriding asynchronous master reset input (MR) and twelve fully buffered outputs (O_0 , O_3 to O_{13}). The counter advances on the HIGH to LOW transition of \overline{CP} . A HIGH on MR clears all counter stages and forces all outputs LOW, independent of the state of \overline{CP} . Each counter stage is a static toggle flip-flop. A feature of the HEF4020B is: high speed (typ. 35 MHz at $V_{DD} = 15\text{ V}$).



- HEF4020BP(N): 16-lead DIL; plastic (SOT38-1)
 - HEF4020BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
 - HEF4020BT(D): 16-lead SO; plastic (SOT109-1)
- (): Package Designator North America

PINNING

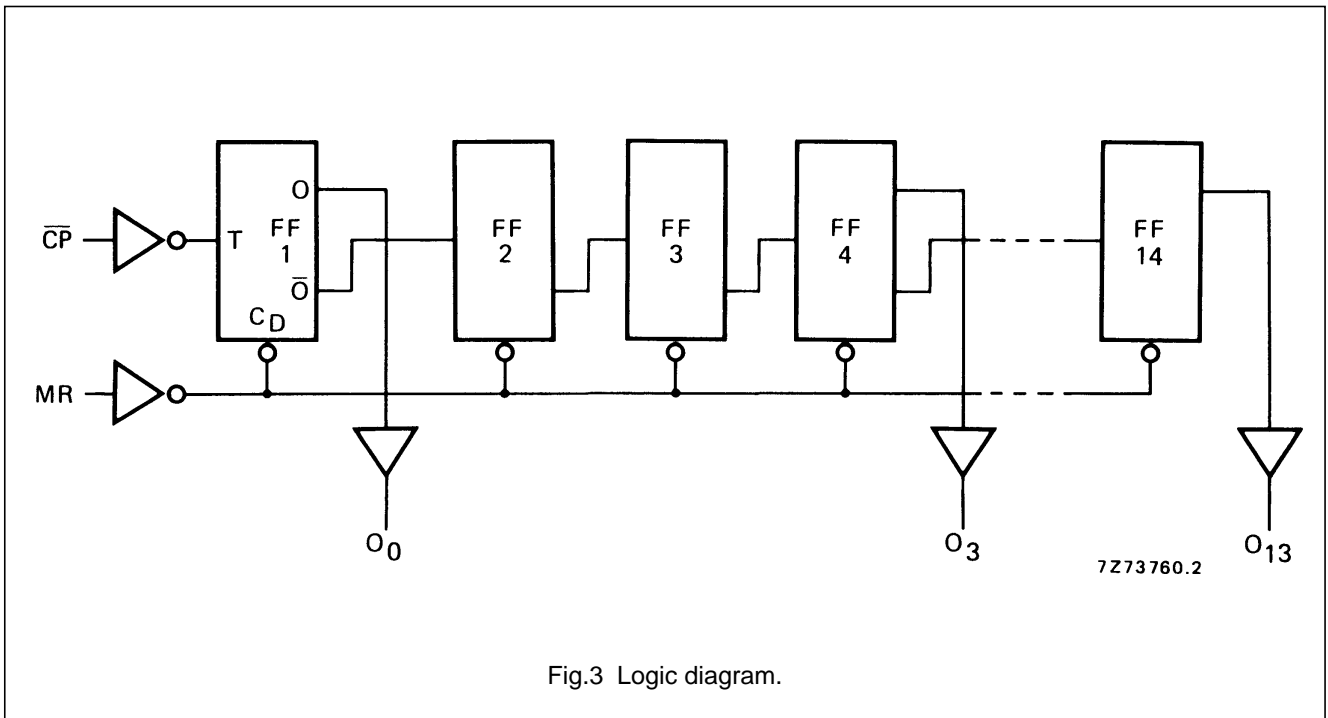
- \overline{CP} clock input (HIGH to LOW edge triggered)
- MR master reset input (active HIGH)
- O_0, O_3 to O_{13} parallel outputs

FAMILY DATA, I_{DD} LIMITS category MSI

See Family Specifications

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MSI**AC CHARACTERISTICS**

$V_{SS} = 0$ V; $T_{amb} = 25$ °C; $C_L = 50$ pF; input transition times ≤ 20 ns; see also waveforms Fig.4

| | V_{DD} V | SYMBOL | MIN. | TYP. | MAX. | TYPICAL EXTRAPOLATION FORMULA | | |
|--|--|------------|-----------|------|------|--|---|--|
| Propagation delays $\overline{CP} \rightarrow O_0$ HIGH to LOW | 5 | t_{PHL} | | 105 | 210 | ns | $78 \text{ ns} + (0,55 \text{ ns/pF}) C_L$ | |
| | 10 | | 45 | 90 | ns | $34 \text{ ns} + (0,23 \text{ ns/pF}) C_L$ | | |
| | 15 | | 30 | 65 | ns | $22 \text{ ns} + (0,16 \text{ ns/pF}) C_L$ | | |
| | LOW to HIGH | 5 | t_{PLH} | | 105 | 210 | ns | $78 \text{ ns} + (0,55 \text{ ns/pF}) C_L$ |
| | | 10 | | 50 | 95 | ns | $39 \text{ ns} + (0,23 \text{ ns/pF}) C_L$ | |
| | | 15 | | 35 | 70 | ns | $27 \text{ ns} + (0,16 \text{ ns/pF}) C_L$ | |
| $O_n \rightarrow O_{n+1}$ HIGH to LOW | 5 | t_{PHL} | | 80 | 160 | ns | $53 \text{ ns} + (0,55 \text{ ns/pF}) C_L$ | |
| | 10 | | 30 | 60 | ns | $19 \text{ ns} + (0,23 \text{ ns/pF}) C_L$ | | |
| | 15 | | 20 | 40 | ns | $12 \text{ ns} + (0,16 \text{ ns/pF}) C_L$ | | |
| | LOW to HIGH | 5 | t_{PLH} | | 70 | 140 | ns | $43 \text{ ns} + (0,55 \text{ ns/pF}) C_L$ |
| | | 10 | | 25 | 50 | ns | $14 \text{ ns} + (0,23 \text{ ns/pF}) C_L$ | |
| | | 15 | | 20 | 40 | ns | $12 \text{ ns} + (0,16 \text{ ns/pF}) C_L$ | |
| MR $\rightarrow O_n$ HIGH to LOW | 5 | t_{PHL} | | 180 | 360 | ns | $153 \text{ ns} + (0,55 \text{ ns/pF}) C_L$ | |
| | 10 | | 90 | 180 | ns | $79 \text{ ns} + (0,23 \text{ ns/pF}) C_L$ | | |
| | 15 | | 70 | 140 | ns | $62 \text{ ns} + (0,16 \text{ ns/pF}) C_L$ | | |
| | Output transition times HIGH to LOW | 5 | t_{THL} | | 60 | 120 | ns | $10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$ |
| | | 10 | | 30 | 60 | ns | $9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$ | |
| | | 15 | | 20 | 40 | ns | $6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$ | |
| LOW to HIGH | 5 | t_{TLH} | | 60 | 120 | ns | $10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$ | |
| | 10 | | 30 | 60 | ns | $9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$ | | |
| | 15 | | 20 | 40 | ns | $6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$ | | |
| Minimum clock pulse width; HIGH | 5 | t_{WCPH} | 50 | 25 | | ns | | |
| | 10 | | 25 | 15 | | ns | | |
| | 15 | | 20 | 10 | | ns | | |
| Minimum MR pulse width; HIGH | 5 | t_{WMRH} | 130 | 65 | | ns | | |
| | 10 | | 95 | 50 | | ns | | |
| | 15 | | 90 | 45 | | ns | | |
| Recovery time for MR | 5 | t_{RMR} | 115 | 60 | | ns | | |
| | 10 | | 65 | 35 | | ns | | |
| | 15 | | 55 | 25 | | ns | | |
| Maximum clock pulse frequency | 5 | f_{max} | 5 | 10 | | MHz | | |
| | 10 | | 13 | 25 | | MHz | | |
| | 15 | | 18 | 35 | | MHz | | |

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| | V_{DD} V | TYPICAL FORMULA FOR P (μ W) | |
|---|---------------|--|--|
| Dynamic power dissipation per package (P) | 5 10 15 | $600 f_i + \sum (f_o C_L) \times V_{DD}^2$ $2\,800 f_i + \sum (f_o C_L) \times V_{DD}^2$ $8\,200 f_i + \sum (f_o C_L) \times V_{DD}^2$ | where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load cap. (pF) $\sum (f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V) |

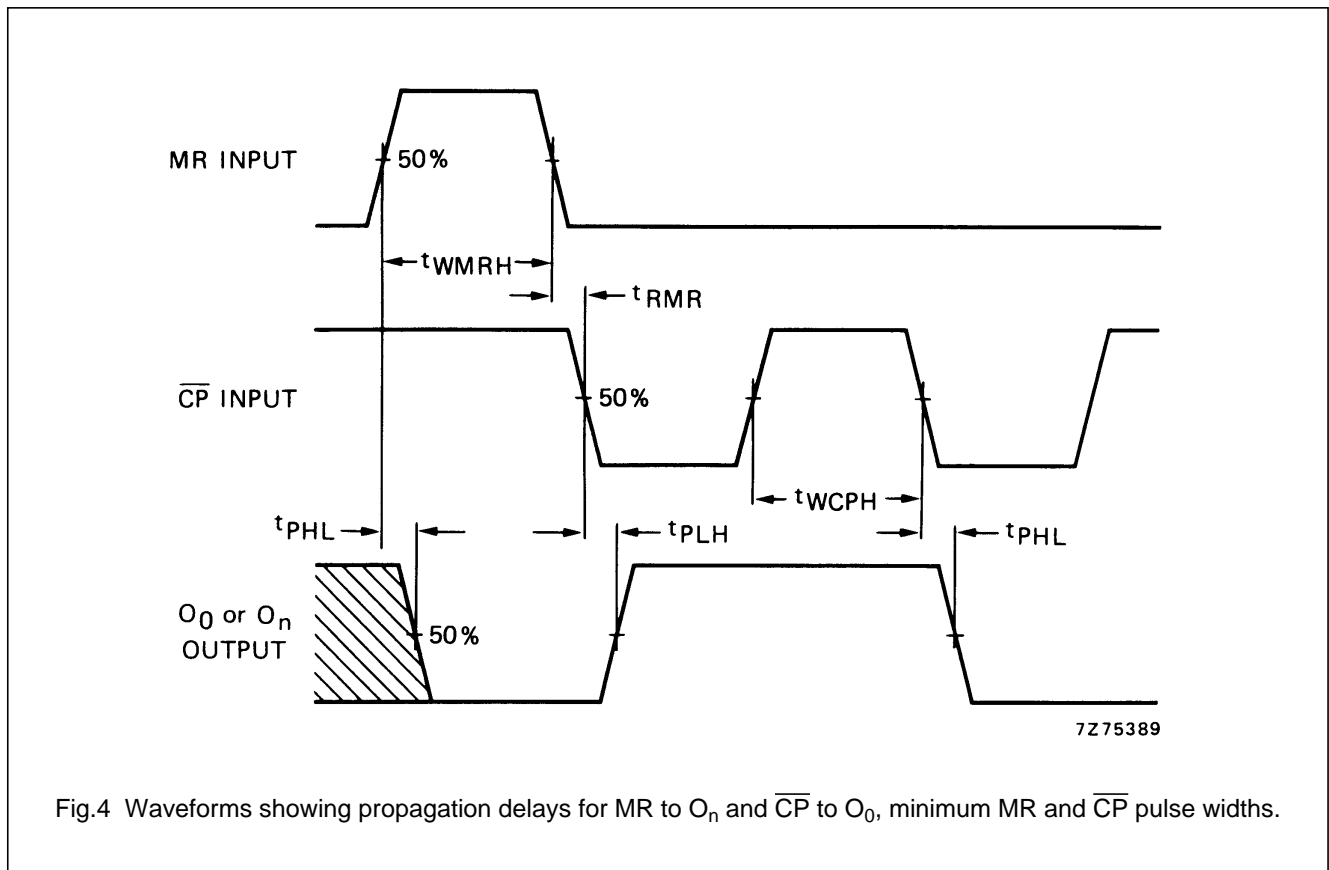
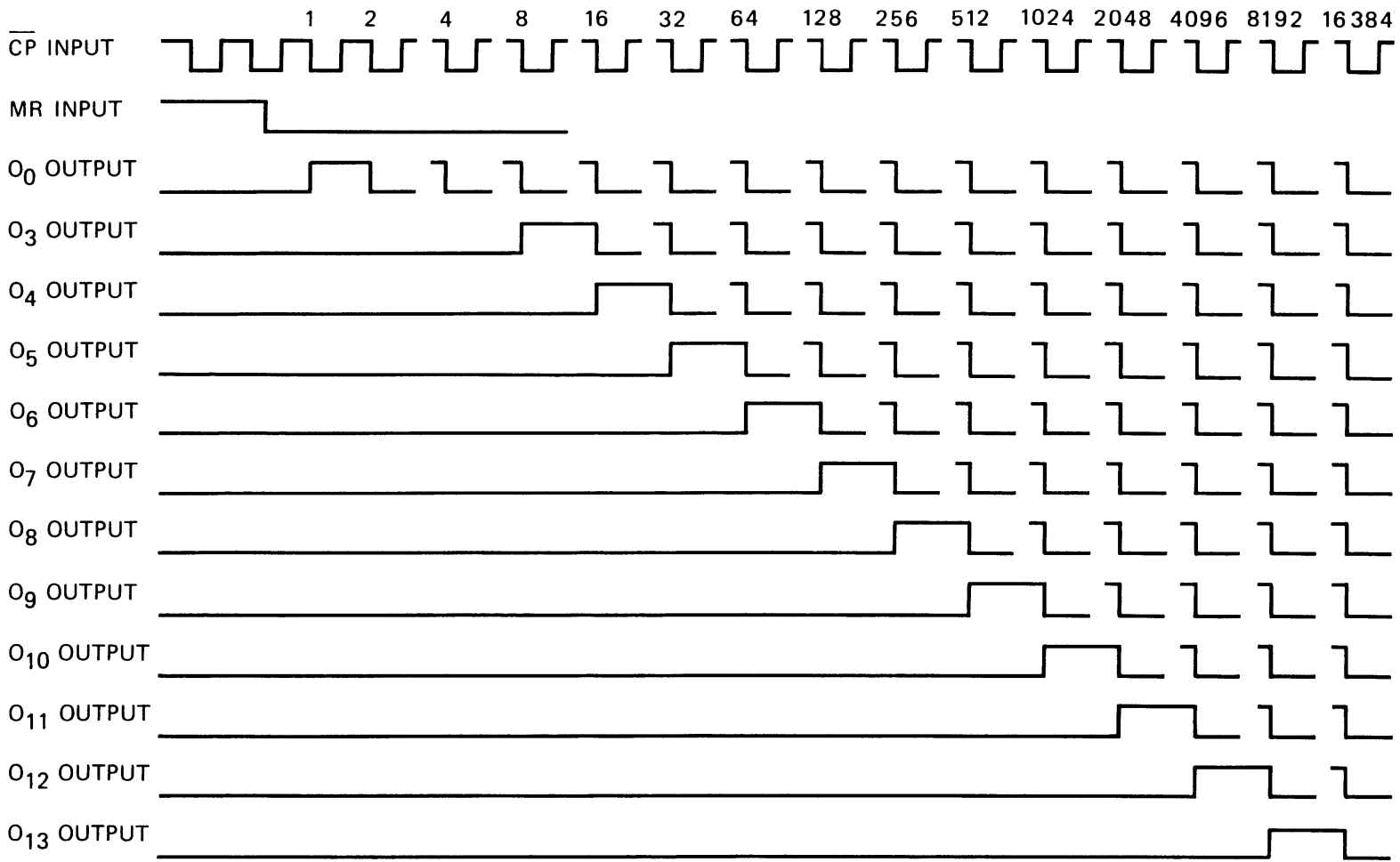


Fig.4 Waveforms showing propagation delays for MR to O_n and \overline{CP} to O_0 , minimum MR and \overline{CP} pulse widths.

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Fig.5 Timing diagram.