MC14568B

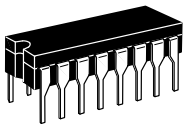
Phase Comparator and Programmable Counters

The MC14568B consists of a phase comparator, a divide–by–4, 16, 64 or 100 counter and a programmable divide–by–N 4–bit binary counter (all positive–edge triggered) constructed with MOS P–channel and N–channel enhancement mode devices (complementary MOS) in a monolithic structure.

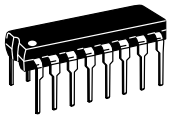
The MC14568B has been designed for use in conjunction with a programmable divide–by–N counter for frequency synthesizers and phase–locked loop applications requiring low power dissipation and/or high noise immunity.

This device can be used with both counters cascaded and the output of the second counter connected to the phase comparator (CTL high), or used independently of the programmable divide–by–N counter, for example cascaded with a MC14569B, MC14522B or MC14526B (CTL low).

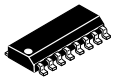
- Supply Voltage Range = 3.0 to 18 V
- Capable of Driving Two Low–Power TTL Loads, One Low–Power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Chip Complexity: 549 FETs or 137 Equivalent Gates



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



D SUFFIX
SOIC
CASE 751B

ORDERING INFORMATION

MC14XXXBCP	Plastic
MC14XXXBCL	Ceramic
MC14XXXBD	SOIC

T_A = – 55° to 125°C for all packages.

MAXIMUM RATINGS* (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	– 0.5 to + 18	Vdc
Input Voltage, All Inputs	V_{in}	– 0.5 to V_{DD} + 0.5	Vdc
DC Input Current, per Pin	I_{in}	± 10	mAdc
Power Dissipation, per Package†	P_D	500	mW
Operating Temperature Range	T_A	– 55 to + 125	°C
Storage Temperature Range	T_{stg}	– 65 to + 150	°C

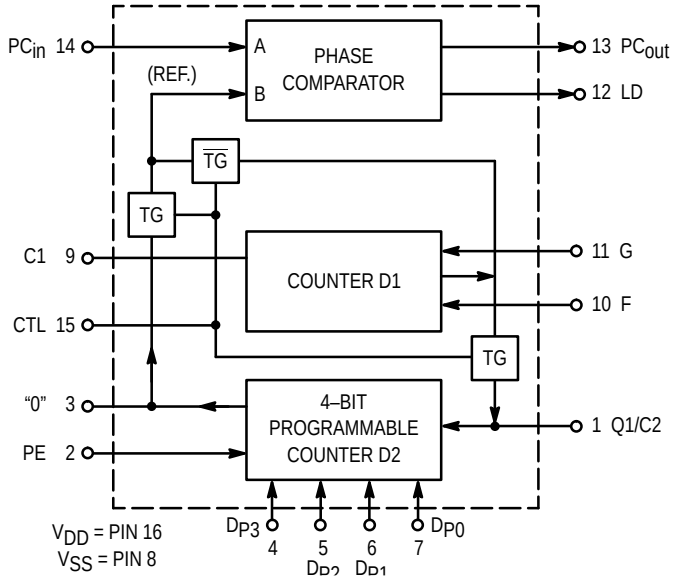
* Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating:
Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C
Ceramic “L” Packages: – 12 mW/°C From 100°C To 125°C

TRUTH TABLE

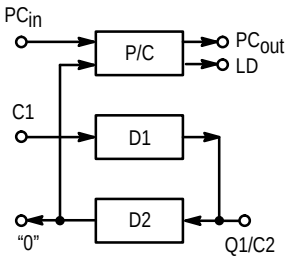
F Pin 10	G Pin 11	Division Ratio of Counter D1
0	0	4
0	1	16
1	0	64
1	1	100

The divide by zero state on the programmable divide–by–N 4–bit binary counter, D2, is illegal.

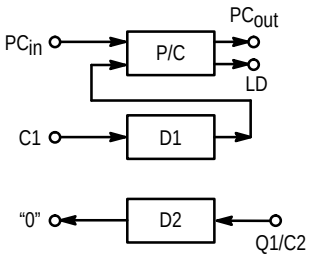
BLOCK DIAGRAM



CTL HIGH



CTL LOW



REV 3
1/94

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	– 55°C Min	– 55°C Max	25°C Min	25°C Typ #	25°C Max	125°C Min	125°C Max	Unit
Output Voltage “0” Level V_{in} = V_{DD} or 0	V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
“1” Level V_{in} = 0 or V_{DD}	V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage#‡ “0” Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	—	1.5	—	2.25	1.5	—	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	—	3.0	—	4.50	3.0	—	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	—	4.0	—	6.75	4.0	—	4.0	
“1” Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	—	3.5	2.75	—	3.5	—	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	—	7.0	5.50	—	7.0	—	
(V_O = 1.5 or 13.5 Vdc)		15	11	—	11	8.25	—	11	—	
Output Drive Current	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	– 1.2	—	– 1.0	– 1.7	—	– 0.7	—	
(V_{OH} = 4.6 Vdc)		5.0	– 0.25	—	– 0.2	– 0.36	—	– 0.14	—	
(V_{OH} = 9.5 Vdc)		10	– 0.62	—	– 0.5	– 0.9	—	– 0.35	—	
(V_{OH} = 13.5 Vdc)		15	– 1.8	—	– 1.5	– 3.5	—	– 1.1	—	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	—	1.3	2.25	—	0.9	—	
(V_{OL} = 1.5 Vdc)		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I_{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	µAdc
Input Capacitance	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package) V_{in} = 0 or V_{DD}, I_{out} = 0 µA	I_{DD}	5.0	—	5.0	—	0.005	5.0	—	150	µAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.2 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (0.4 µA/kHz) f + I_{DD}							
		15	I_T = (0.9 µA/kHz) f + I_{DD}							
Three–State Leakage Current Pins 1, 13	I_{TL}	15	—	±0.1	—	±0.0001	±0.1	—	±3.0	µAdc

#Noise immunity for worst input combination.

Noise Margin for both “1” and “0” level = 1.0 V min @ V_{DD} = 5.0 V
2.0 V min @ V_{DD} = 10 V
2.5 V min @ V_{DD} = 15 V

†To calculate total supply current at loads other than 50 pF:

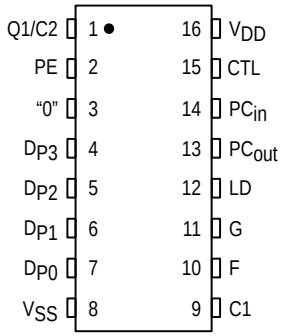
$$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50)\ V_{DD} f$$

where: I_T is in µA (per package), C_L in pF, V_{DD} in V, and f in kHz is input frequency.

** The formulas given are for the typical characteristics only at 25°C.

‡Pin 15 is connected to V_{SS} or V_{DD} for input voltage test.

PIN ASSIGNMENT



SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} V	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}	5.0 10 15	— — —	180 90 65	360 180 130	ns
Output Fall Time	t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Minimum Pulse Width, C1, Q1/C2, or PC_{in} Input	t_{WH}	5.0 10 15	— — —	125 60 45	250 120 90	ns
Maximum Clock Rise and Fall Time, C1, Q1/C2, or PC_{in} Input	t_{TLH}, t_{THL}	5.0 10 15	15 15 15	— — —	— — —	µs
PHASE COMPARATOR						
Input Resistance	R_{in}	5.0 to 15	—	10^6	—	MΩ
Input Sensitivity, dc Coupled	—	5.0 to 15	See Input Voltage			
Turn–Off Delay Time, PC_{out} and LD Outputs	t_{PHL}	5.0 10 15	— — —	550 195 120	1100 390 240	ns
Turn–On Delay Time. PC_{out} and LD Outputs	t_{PLH}	5.0 10 15	— — —	675 300 190	1350 600 380	ns
DIVIDE–BY–4, 16, 64 OR 100 COUNTER (D1)						
Maximum Clock Pulse Frequency	f_{cl}					MHz
Division Ratio = 4, 64 or 100		5.0 10 15	3.0 8.0 10	6.0 16 22	— — —	
Division Ratio = 16		5.0 10 15	1.0 3.0 5 0	2.5 6.3 9.7	— — —	
Propagation Delay Time, Q1/C2 Output	t_{PLH}, t_{PHL}					ns
Division Ratio = 4, 64 or 100		5.0 10 15	— — —	450 190 130	900 380 260	
Division Ratio = 16		5.0 10 15	— — —	720 300 200	1440 600 400	
PROGRAMMABLE DIVIDE–BY–N 4–BIT COUNTER (D2)						
Maximum Clock Pulse Frequency (Figure 3a)	f_{cl}	5.0 10 15	1.2 3.0 4.0	1.8 8.5 12	— — —	MHz
Turn–On Delay Time, “0” Output (Figure 3a)	t_{PLH}	5.0 10 15	— — —	450 190 130	900 380 260	ns
Turn–Off Delay Time, “0” Output (Figure 3a)	t_{PHL}	5.0 10 15	— — —	225 85 60	450 170 150	ns
Minimum Preset Enable Pulse Width	$t_{WH(PE)}$	5.0 10 15	— — —	75 40 30	250 100 75	ns

SWITCHING TIME TEST CIRCUITS AND WAVEFORMS

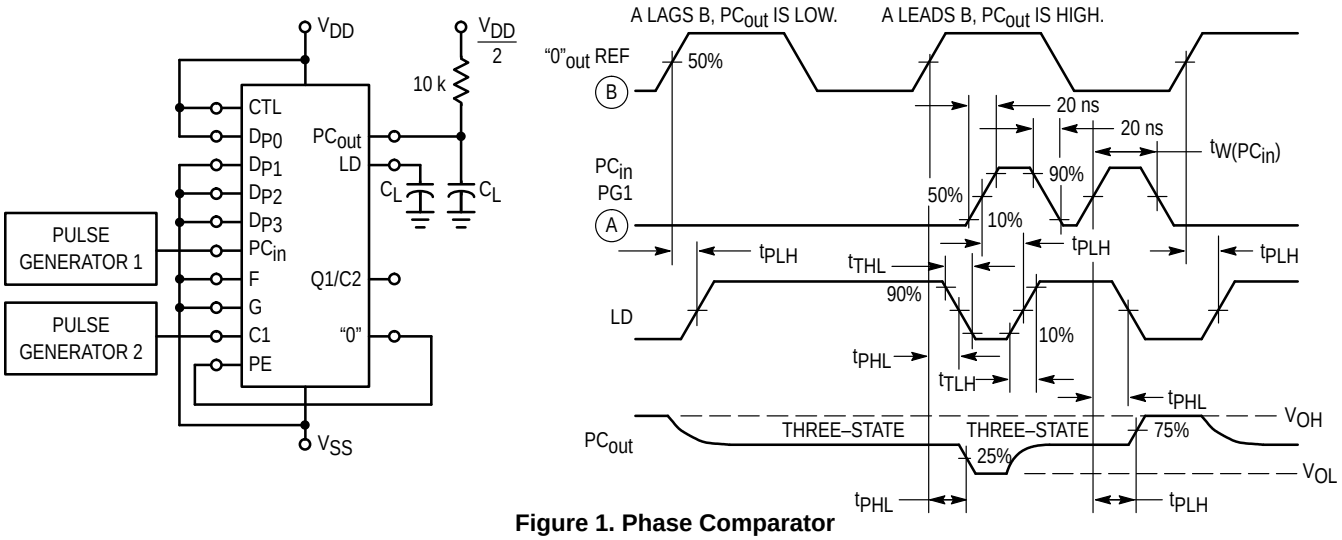


Figure 1. Phase Comparator

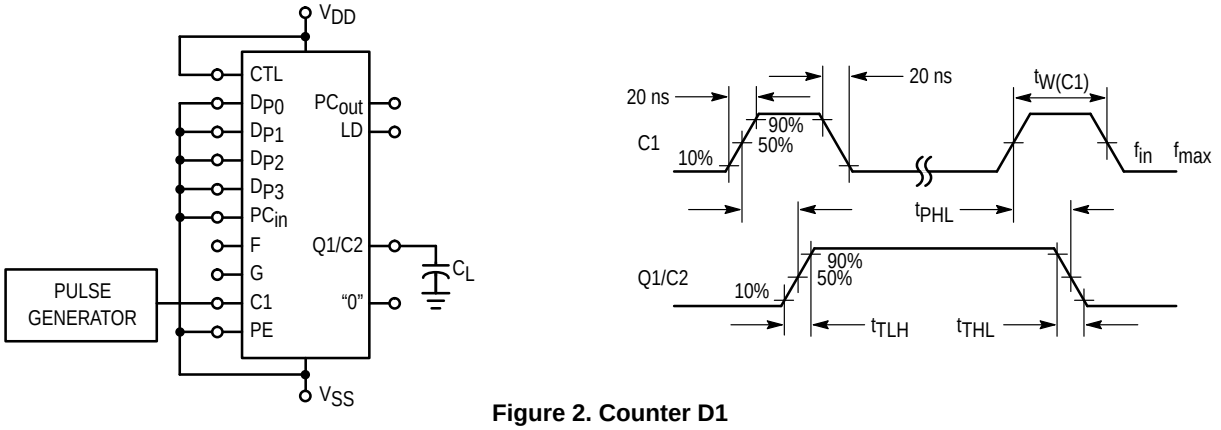
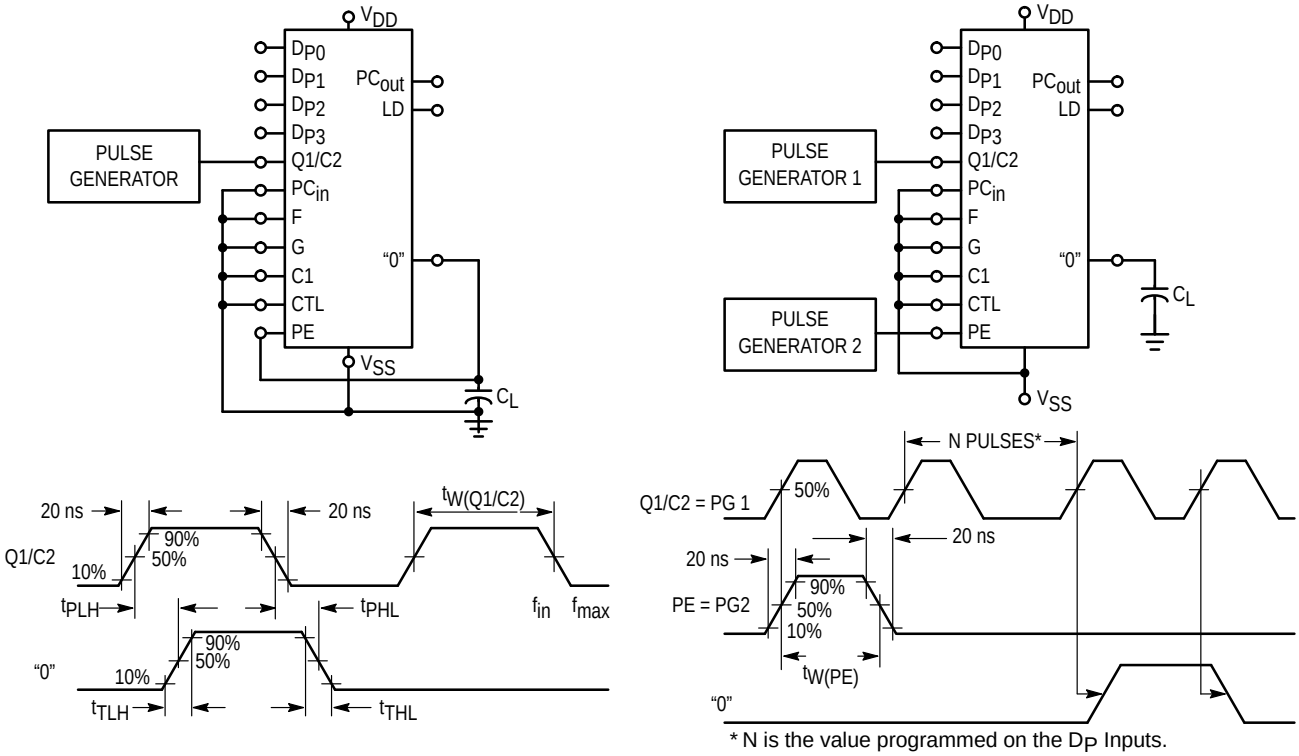


Figure 2. Counter D1



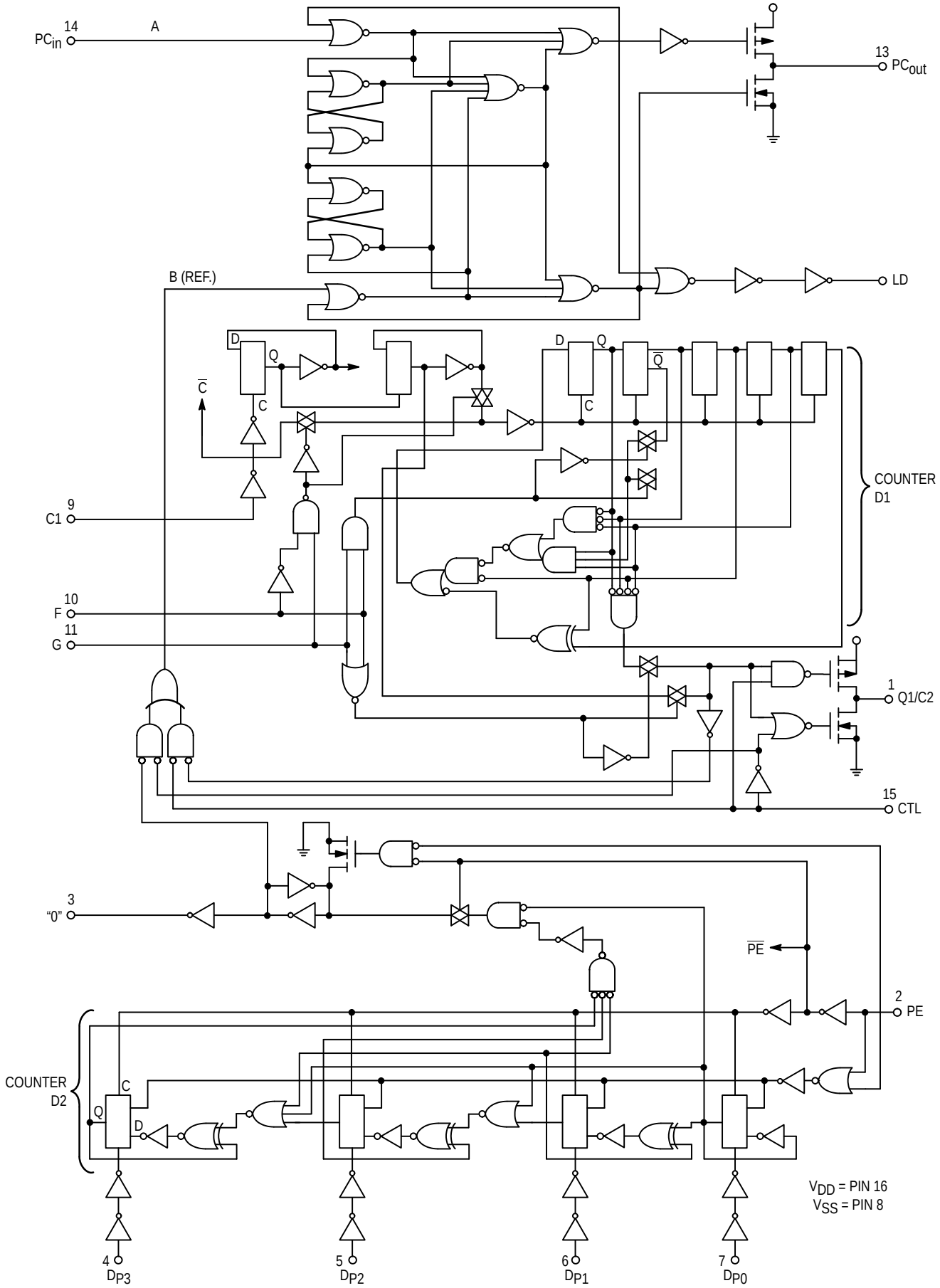
a.

b.

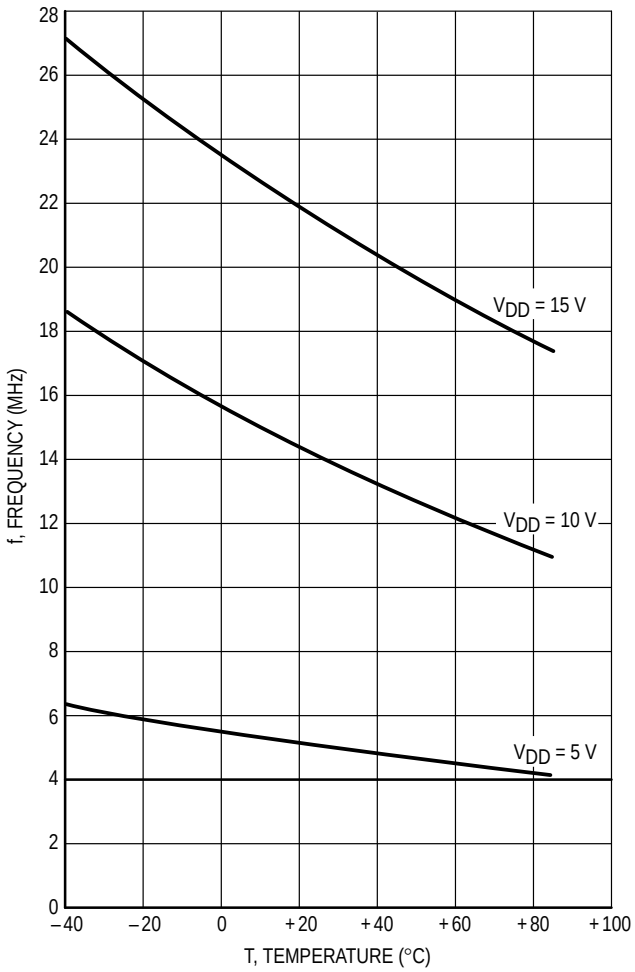
* N is the value programmed on the D_P Inputs.

Figure 3. Counter D2

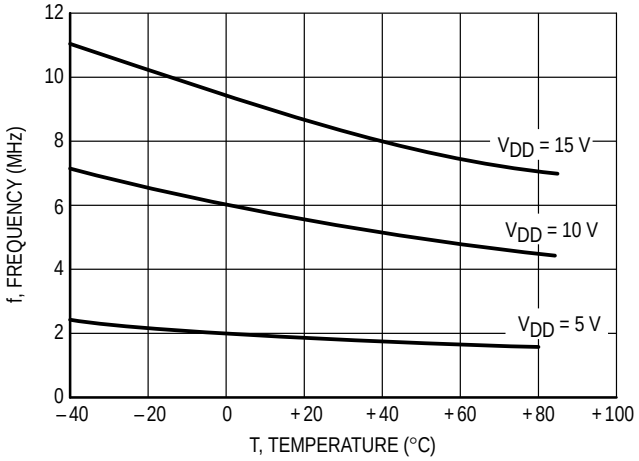
LOGIC DIAGRAM



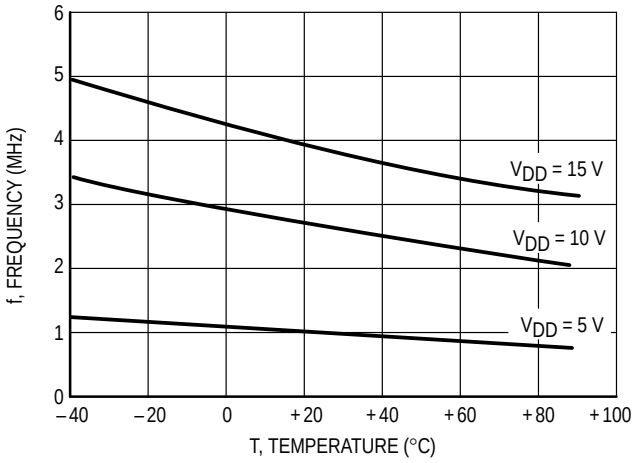
Typical Maximum Frequency Divider D1
Division ratios: 4, 64 or 100 (C_L = 50 pF)



Typical Maximum Frequency Divider D1
Division ratio: 16 (C_L = 50 pF)



Typical Maximum Frequency Divider D2
Division ratio: 2 (C_L = 50 pF)



OPERATING CHARACTERISTICS

The MC14568B contains a phase comparator, a fixed divider (÷ 4, ÷ 16, ÷ 64, ÷ 100) and a programmable divide–by–N 4–bit counter.

PHASE COMPARATOR

The phase comparator is a positive edge controlled logic circuit. It essentially consists of four flip–flops and an output pair of MOS transistors. Only one of its inputs (PC_{in}, pin 14) is accessible externally. The second is connected to the output of one of the two counters D1 or D2 (see block diagram).

Duty cycles of both input signals (at A and B) need not be taken into consideration since the comparator responds to leading edges only.

If both input signals have identical frequencies but different phases, with signal A (pin 14) leading signal B (Ref.), the comparator output will be high for the time equal to the phased difference.

If signal A lags signal B, the output will be low for the same time. In between, the output will be in a three–state condition and the voltage on the capacitor of an RC filter normally connected at this point will have some intermediate value (see Figure 4). When used in a phase locked loop, this value will adjust the Voltage Controlled Oscillator frequency by reducing the phase difference between the reference signal and the divided VCO frequency to zero.

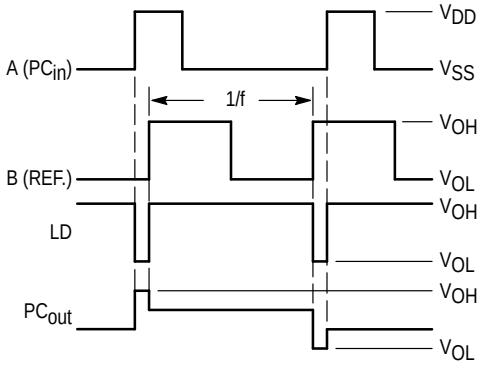


Figure 4. Phase Comparator Waveforms

If the input signals have different frequencies, the output signal will be high when signal B has a lower frequency than signal A, and low otherwise.

Under the same conditions of frequency difference, the output will vary between V_{OH} (or V_{OL}) and some intermediate value until the frequencies of both signals are equal and their phase difference equal to zero, i.e. until locked condition is obtained.

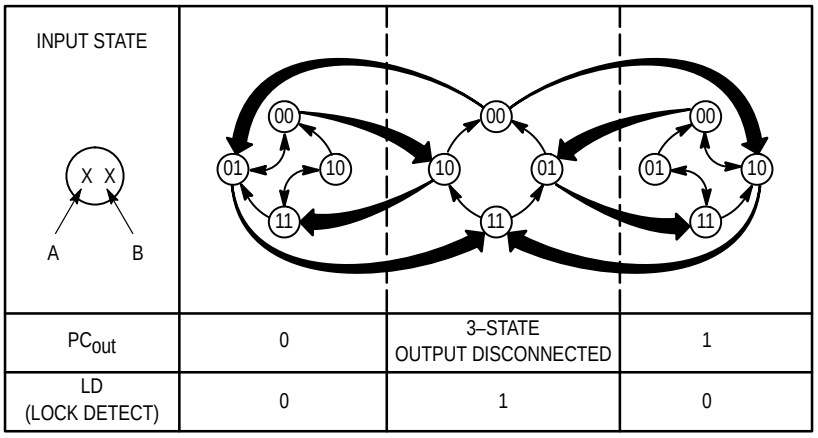
Capture and lock range will be determined by the VCO frequency range. The comparator is provided with a lock indicator output, which will stay at logic 1 in locked conditions.

The state diagram (Figure 5) depicts the internal state transitions. It assumes that only one transition on either signal occurs at any time. It shows that a change of the output state is always associated with a positive transition of either signal. For a negative transition, the output does not change state. A positive transition may not cause the output to change, this happens when the signals have different frequencies.

DIVIDE BY 4, 16, 64 OR 100 COUNTER (D1)

This counter is able to work at an input frequency of 5 MHz for a V_{DD} value of 10 volts over the standard temperature range when dividing by 4, 64 and 100. Programming is accomplished by use of inputs F and G (pins 10 and 11) according to the truth table shown. Connecting the Control input (CTL, pin 15), to V_{DD} allows cascading this counter with the programmable divide–by–N counter provided in the same package. Independent operation is obtained when the Control input is connected to V_{SS}.

The different division ratios have been chosen to generate the reference frequencies corresponding to the channel spacings normally required in frequency synthesizer applications. For example. with the division ratio 100 and a 5 MHz crystal stabilized source a reference frequency of 50 kHz is supplied to the comparator. The lower division ratios permit operation with low frequency crystals.



PC_{out}	0	3–STATE OUTPUT DISCONNECTED	1
LD (LOCK DETECT)	0	1	0

Figure 5. Phase Comparator State Diagram

If used in cascade with the programmable divide–by–N counter, practically all usual reference frequencies, or channel spacings of 25, 20, 12.5, 10, 6.25 kHz, etc. are easily achievable.

PROGRAMMABLE DIVIDE–BY–N 4–BIT COUNTER (D2)

This counter is programmable by using inputs D_{P0} ... D_{P3} (pins 7 ... 4). The Preset Enable input enables the parallel preset inputs D_{P0}... D_{P3}. The “0” output must be externally connected to the PE input for single stage applications. Since there is not a cascade feedback input, this counter, when cascaded, must be used as the most significant digit. Because of this, it can be cascaded with binary counters as well as with BCD counters (MC14569B, MC14522B, MC14526B).

TYPICAL APPLICATIONS

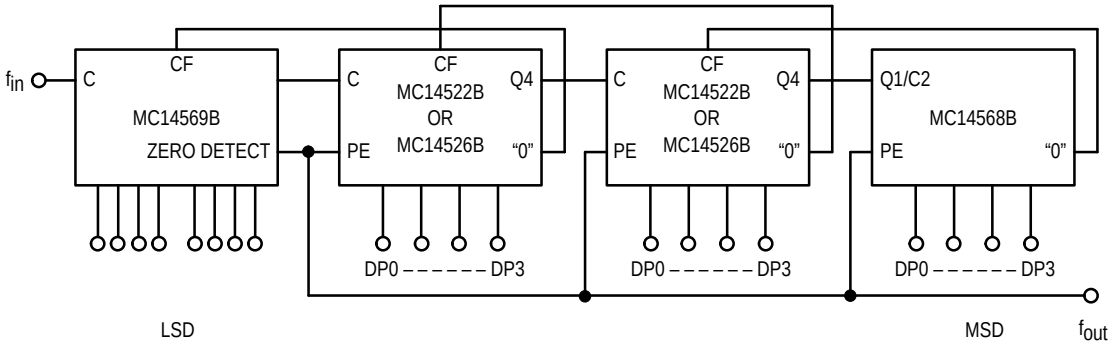
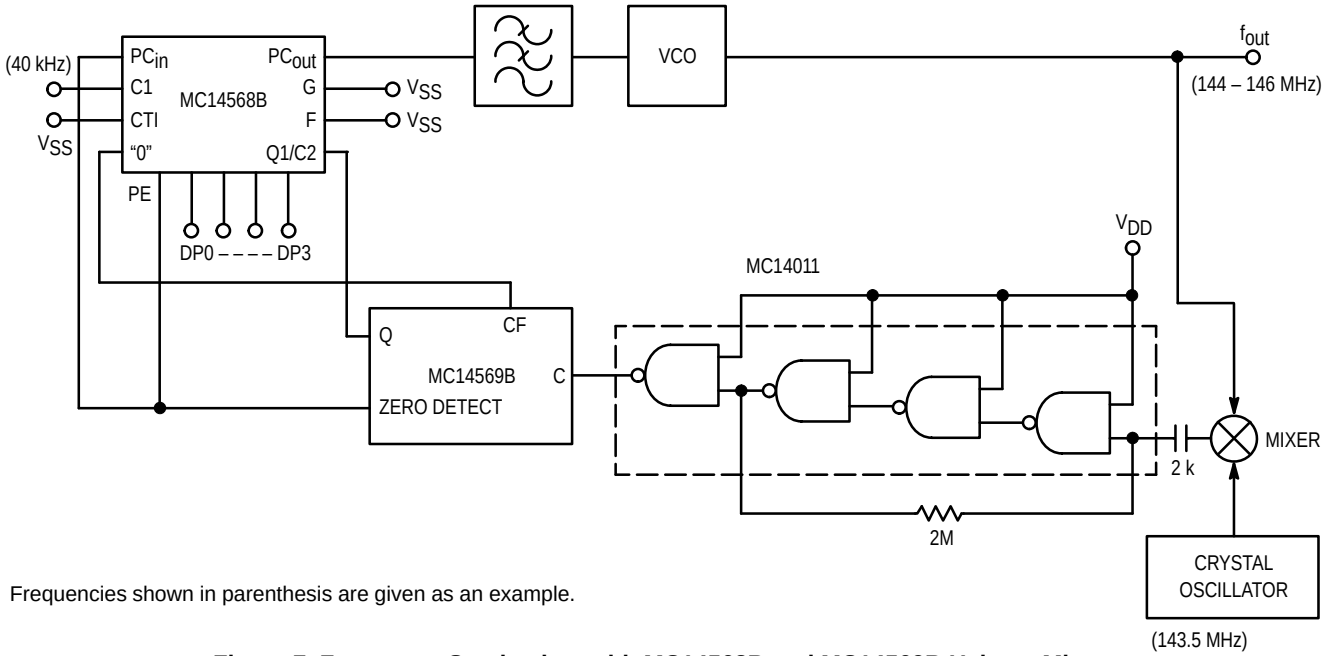
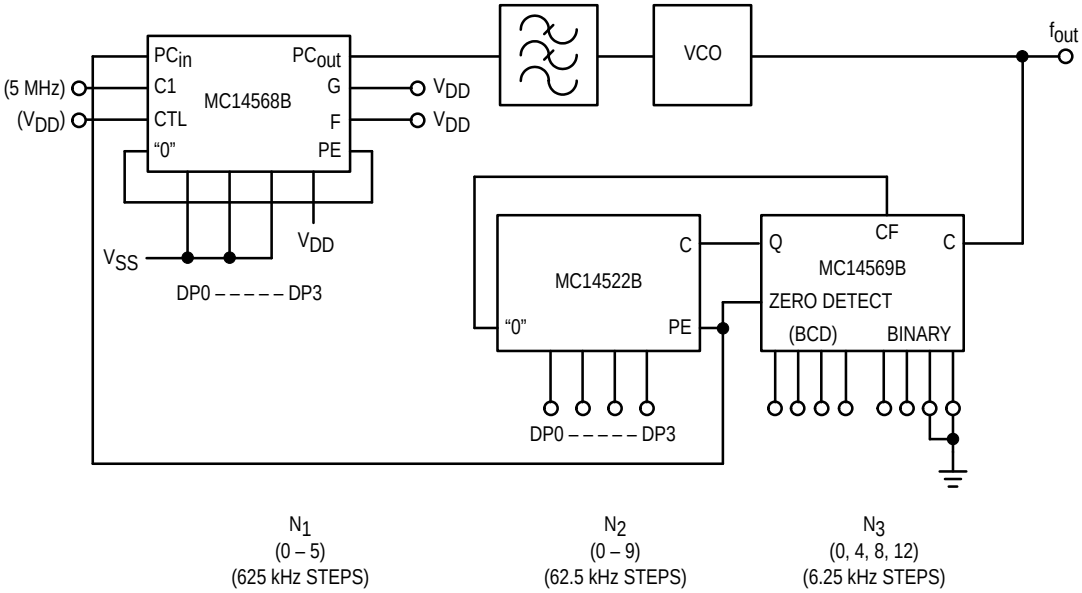


Figure 6. Cascading MC14568B and MC14522B or MC14526B with MC14569B



Frequencies shown in parenthesis are given as an example.

Figure 7. Frequency Synthesizer with MC14568B and MC14569B Using a Mixer (Channel Spacing 10 kHz)



Divide ratio = $160N_1 + 16N_2 + N_3$

Example:

$f_{out} = N_1$ (MHz) + N_2 (x 100 kHz) + N_3 (x25 kHz)

Frequency range = 5 MHz

Channel spacing = 25 kHz

Reference frequency = 6.25 kHz

Figures shown in parenthesis refer to example.

Recommended reading:

(1) AN535: "Phase–Lock Techniques"

(2) AR254: "Phase–Locked Loop Design Articles"

Figure 8. Frequency Synthesizer Using MC14568B, MC14569B and MC14522B (Without Mixer)

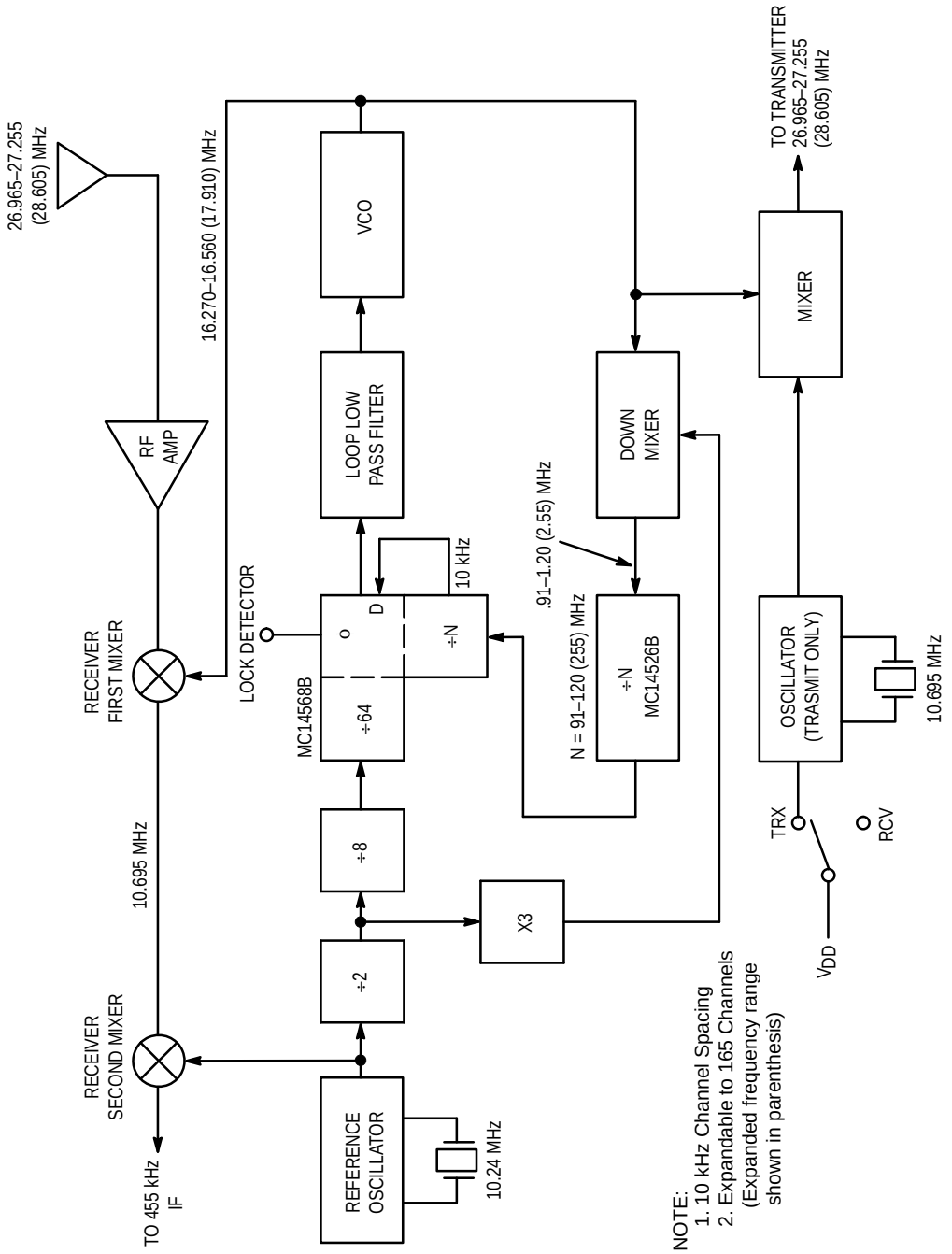
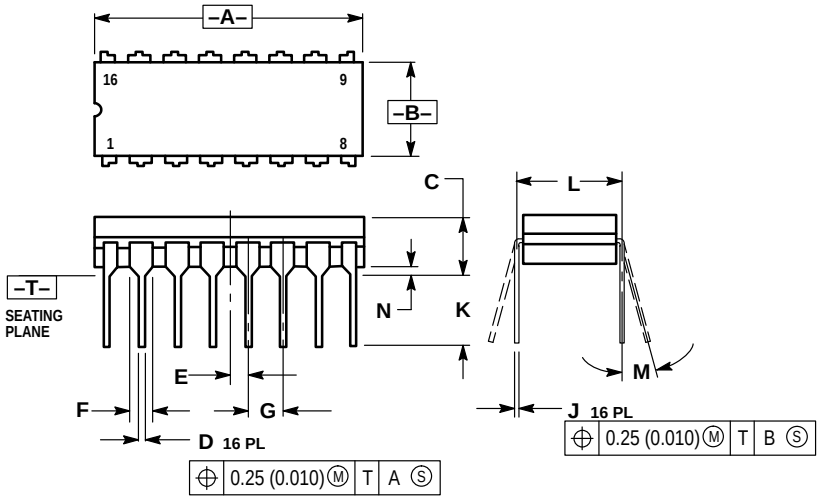


Figure 9. Typical 23–Channel CB Frequency Synthesizer for Double Conversion Transceivers

OUTLINE DIMENSIONS

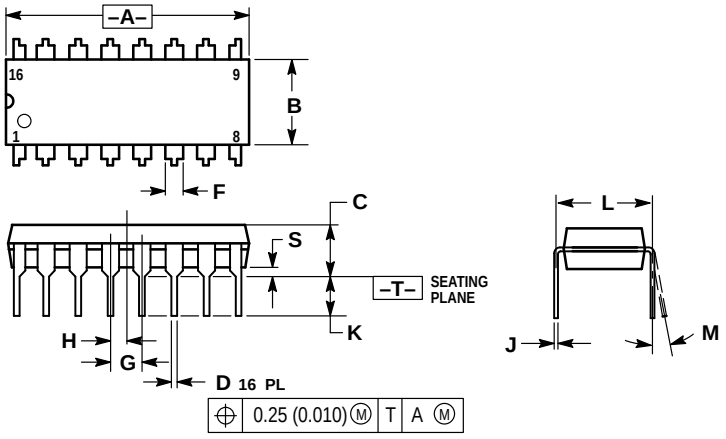
L SUFFIX
CERAMIC DIP PACKAGE
CASE 620–10
ISSUE V



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0 °	15 °	0 °	15 °
N	0.020	0.040	0.51	1.01

P SUFFIX
PLASTIC DIP PACKAGE
CASE 648–08
ISSUE R

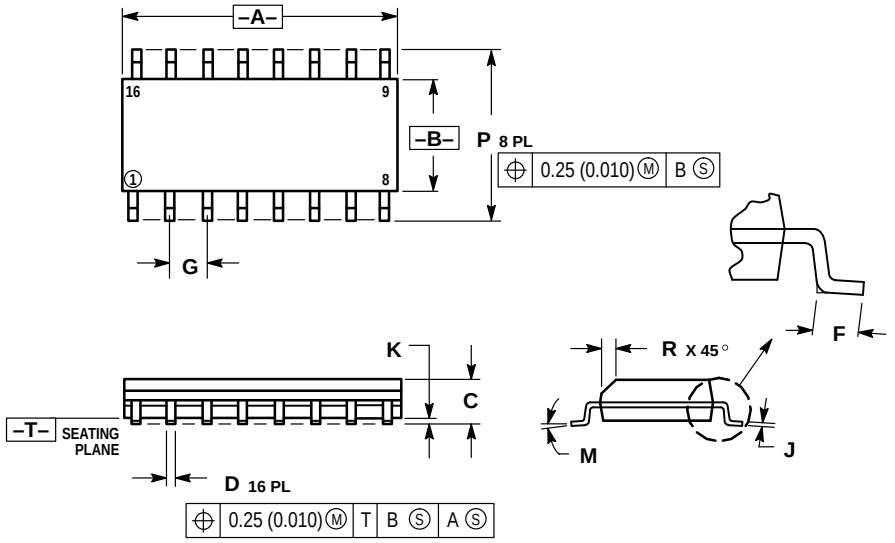


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0 °	10 °	0 °	10 °
S	0.020	0.040	0.51	1.01

OUTLINE DIMENSIONS

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B–05
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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