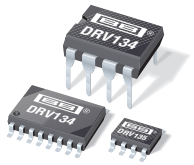


DRV134
DRV135

SBOS094A – JANUARY 1998 – REVISED APRIL 2007

AUDIO BALANCED LINE DRIVERS

FEATURES

- **BALANCED OUTPUT**
- **LOW DISTORTION: 0.0005% at f = 1kHz**
- **WIDE OUTPUT SWING: 17Vrms into 600Ω**
- **HIGH CAPACITIVE LOAD DRIVE**
- **HIGH SLEW RATE: 15V/μs**
- **WIDE SUPPLY RANGE: ±4.5V to ±18V**
- **LOW QUIESCENT CURRENT: ±5.2mA**
- **8-PIN DIP, SO-8, AND SOL-16 PACKAGES**
- **COMPANION TO AUDIO DIFFERENTIAL LINE RECEIVERS: INA134 and INA137**
- **IMPROVED REPLACEMENT FOR SSM2142**

APPLICATIONS

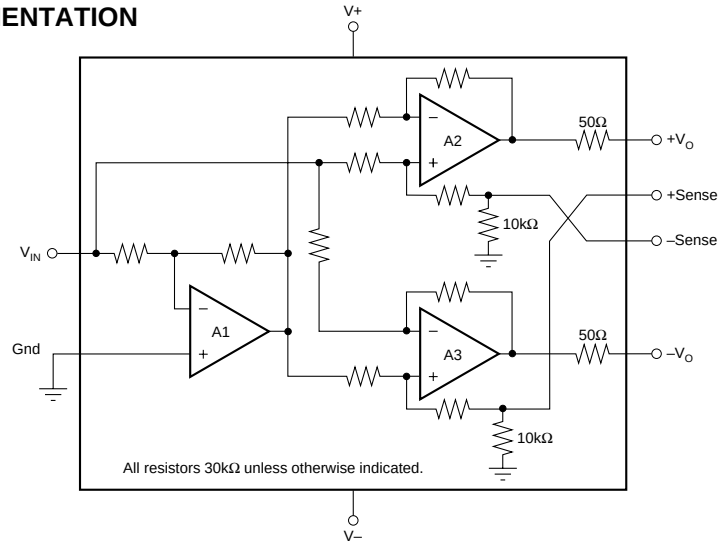
- **AUDIO DIFFERENTIAL LINE DRIVERS**
- **AUDIO MIX CONSOLES**
- **DISTRIBUTION AMPLIFIERS**
- **GRAPHIC/PARAMETRIC EQUALIZERS**
- **DYNAMIC RANGE PROCESSORS**
- **DIGITAL EFFECTS PROCESSORS**
- **TELECOM SYSTEMS**
- **HI-FI EQUIPMENT**
- **INDUSTRIAL INSTRUMENTATION**

DESCRIPTION

The DRV134 and DRV135 are differential output amplifiers that convert a single-ended input to a balanced output pair. These balanced audio drivers consist of high performance op amps with on-chip precision resistors. They are fully specified for high performance audio applications and have excellent ac specifications, including low distortion (0.0005% at 1kHz) and high slew rate (15V/μs).

The on-chip resistors are laser-trimmed for accurate gain and optimum output common-mode rejection. Wide output voltage swing and high output drive capability allow use in a wide variety of demanding applications. They easily drive the large capacitive loads associated with long audio cables. Used in combination with the INA134 or INA137 differential receivers, they offer a complete solution for transmitting analog audio signals without degradation.

The DRV134 is available in 8-pin DIP and SOL-16 surface-mount packages. The DRV135 comes in a space-saving SO-8 surface-mount package. Both are specified for operation over the extended industrial temperature range, –40°C to +85°C and operate from –55°C to +125°C.



SPECIFICATIONS: $V_S = \pm 18V$

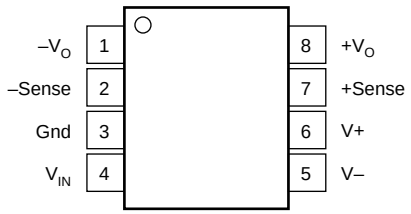
At T_A = +25°C, V_S = ±18V, R_L = 600Ω differential connected between $+V_O$ and $-V_O$, unless otherwise noted.

PARAMETER		CONDITIONS	DRV134PA, UA DRV135UA MIN	TYP	MAX	UNITS
AUDIO PERFORMANCE						
Total Harmonic Distortion + Noise	THD+N	f = 20Hz to 20kHz, V_O = 10Vrms		0.001		%
		f = 1kHz, V_O = 10Vrms		0.0005		%
Noise Floor, RTO[1]		20kHz BW		–98		dBu
Headroom, RTO[1]		THD+N < 1%		+27		dBu
INPUT						
Input Impedance[2]	Z_{IN}			10		kΩ
Input Current	I_{IN}	V_{IN} = ±7.07V		±700	±1000	µA
GAIN		$[(+V_O) - (-V_O)]/V_{IN}$				
Differential		V_{IN} = ±10V				
Initial			5.8	6		dB
Error				±0.1	±2	%
vs Temperature				±10		ppm/°C
Single-Ended		V_{IN} = ±5V				
Initial			5.8	6		dB
Error				±0.7	±2	%
vs Temperature				±10		ppm/°C
Nonlinearity				0.0003		% of FS
OUTPUT						
Common-Mode Rejection, f = 1kHz	OCMR	See OCMR Test Circuit, Figure 4	46	68		dB
Signal Balance Ratio, f = 1kHz	SBR	See SBR Test Circuit, Figure 5	35	54		dB
Output Offset Voltage						
Offset Voltage, Common-Mode	V_{OCM}[3]	V_{IN} = 0		±50	±250	mV
vs Temperature				±150		µV/°C
Offset Voltage, Differential	V_{OD}[4]	V_{IN} = 0		±1	±10	mV
vs Temperature				±5		µV/°C
vs Power Supply	PSRR	V_S = ±4.5V to ±18V	80	110		dB
Output Voltage Swing, Positive		No Load[5]	(V+) – 3	(V+) – 2.5		V
Negative		No Load[5]	(V–) + 2	(V–) + 1.5		V
Impedance				50		Ω
Load Capacitance, Stable Operation	C_L	C_L Tied to Ground (each output)		1		µF
Short-Circuit Current	I_{SC}			±85		mA
FREQUENCY RESPONSE						
Small-Signal Bandwidth				1.5		MHz
Slew Rate	SR			15		V/µs
Settling Time: 0.01%		V_{OUT} = 10V Step		2.5		µs
Overload Recovery		Output Overdriven 10%		3		µs
POWER SUPPLY						
Rated Voltage	V_S			±18		V
Voltage Range			±4.5		±18	V
Quiescent Current	I_Q	I_O = 0		±5.2	±5.5	mA
TEMPERATURE RANGE						
Specification Range			–40		+85	°C
Operation Range			–55		+125	°C
Storage Range			–55		+125	°C
Thermal Resistance	θ_{JA}					
8-Pin DIP				100		°C/W
SO-8 Surface Mount				150		°C/W
SOL-16 Surface Mount				80		°C/W

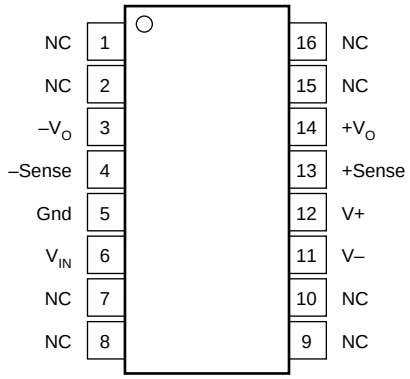
NOTES: (1) dBu = 20log (Vrms/0.7746); RTO = Referred-to-Output.
(2) Resistors are ratio matched but have ±20% absolute value.
(3) $V_{OCM} = [(+V_O) + (-V_O)]/2$. (4) $V_{OD} = (+V_O) - (-V_O)$. (5) Ensures linear operation. Includes common-mode offset.

PIN CONFIGURATIONS

Top View **8-Pin DIP/SO-8**



Top View **SOL-16**



ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage, V+ to V–	40V
Input Voltage Range	V– to V+
Output Short-Circuit (to ground)	Continuous
Operating Temperature	–55°C to +125°C
Storage Temperature	–55°C to +125°C
Junction Temperature	+150°C

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

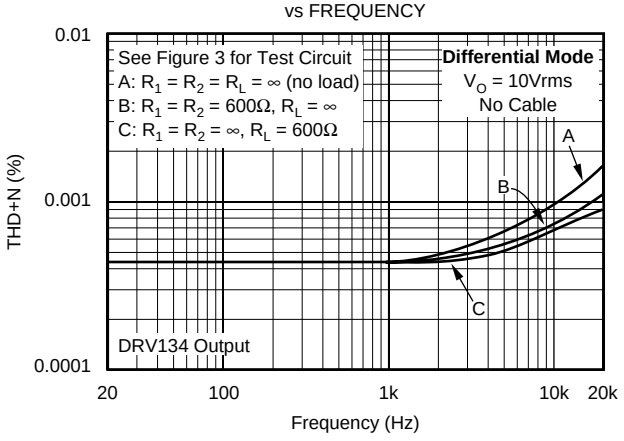
PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
DRV134PA	DIP-8	P	–40°C to +85°C	DRV134PA	Rails, 50
DRV134UA	SOL-16 Surface Mount	DW	–40°C to +85°C	DRV134UA	Rails, 48
"	"	"	"	DRV134UA/1K	Tape and Reel. 1000
DRV135UA	SO-8 Surface Mount	D	–40°C to +85°C	DRV135UA	Rails, 100
"	"	"	"	DRV135UA/2K5	Tape and Reel, 2500

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or see the TI wwebsite at www.ti.com.

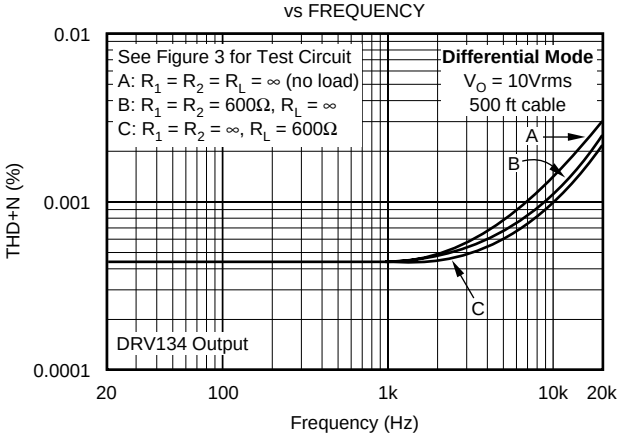
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V_S = ±18V, R_L = 600Ω differential connected between $+V_O$ and $-V_O$, unless otherwise noted.

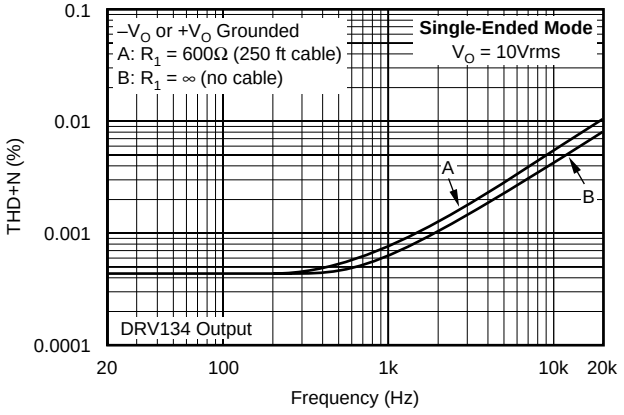
TOTAL HARMONIC DISTORTION+NOISE
vs FREQUENCY



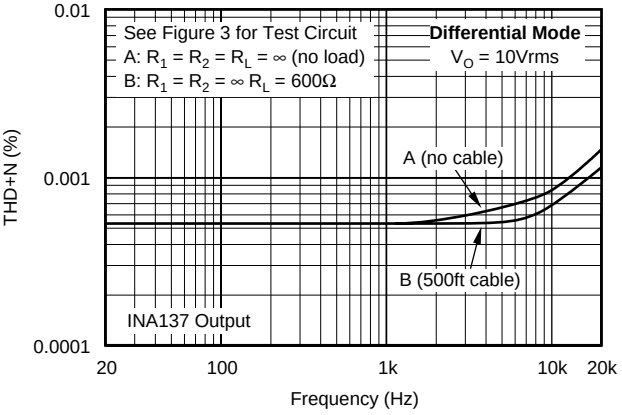
TOTAL HARMONIC DISTORTION+NOISE
vs FREQUENCY



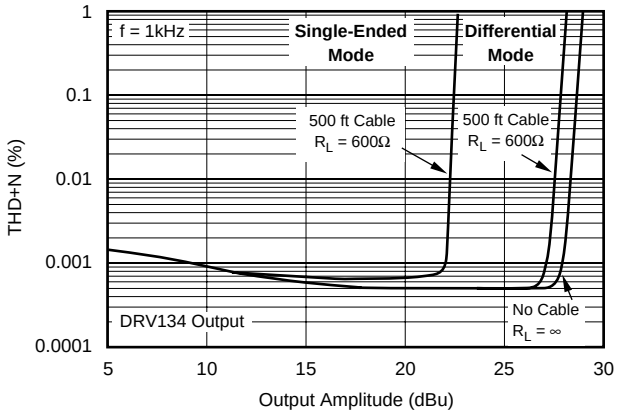
TOTAL HARMONIC DISTORTION+NOISE
vs FREQUENCY



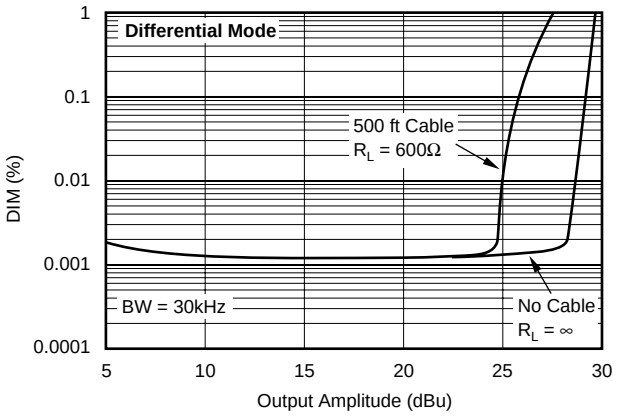
SYSTEM TOTAL HARMONIC DISTORTION+NOISE
vs FREQUENCY



HEADROOM—TOTAL HARMONIC DISTORTION+NOISE
vs OUTPUT AMPLITUDE



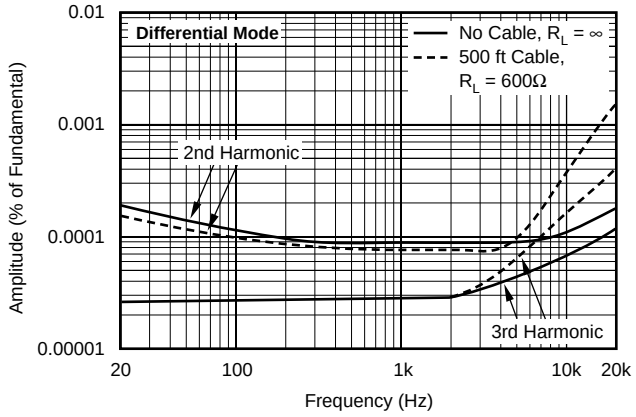
DIM INTERMODULATION DISTORTION
vs OUTPUT AMPLITUDE



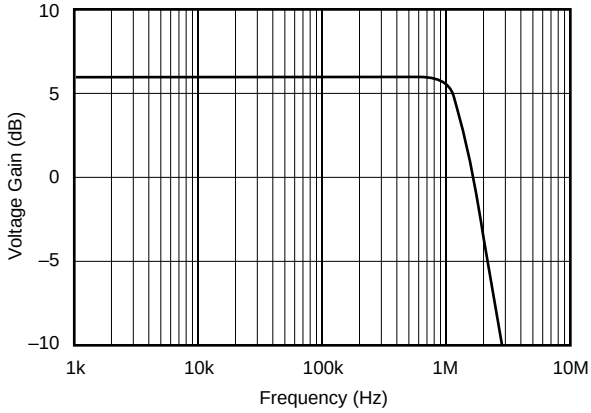
TYPICAL PERFORMANCE CURVES (Cont.)

At T_A = +25°C, V_S = ±18V, R_L = 600Ω differential connected between $+V_O$ and $-V_O$, unless otherwise noted.

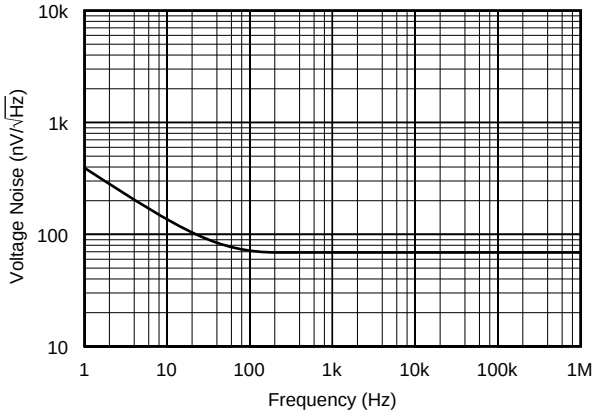
HARMONIC DISTORTION PRODUCTS vs FREQUENCY



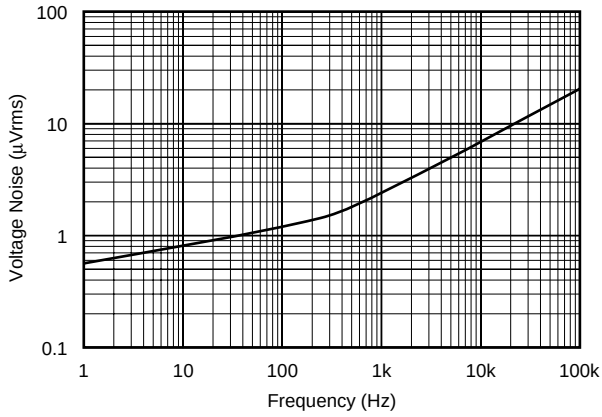
GAIN vs FREQUENCY



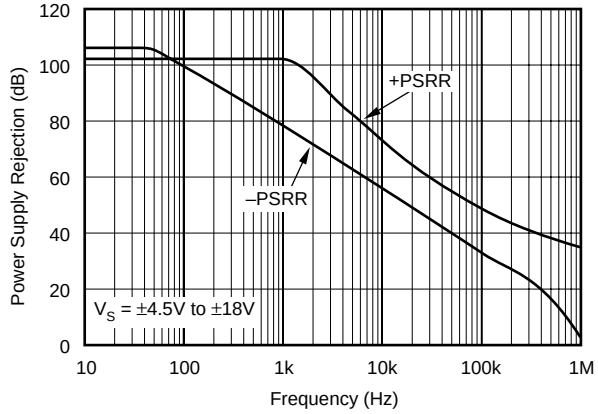
OUTPUT VOLTAGE NOISE SPECTRAL DENSITY vs FREQUENCY



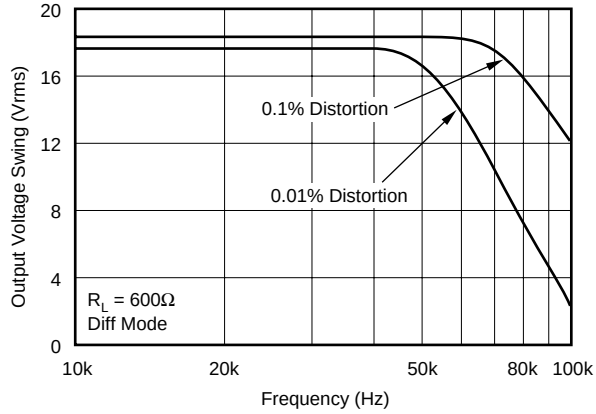
OUTPUT VOLTAGE NOISE vs NOISE BANDWIDTH



POWER SUPPLY REJECTION vs FREQUENCY



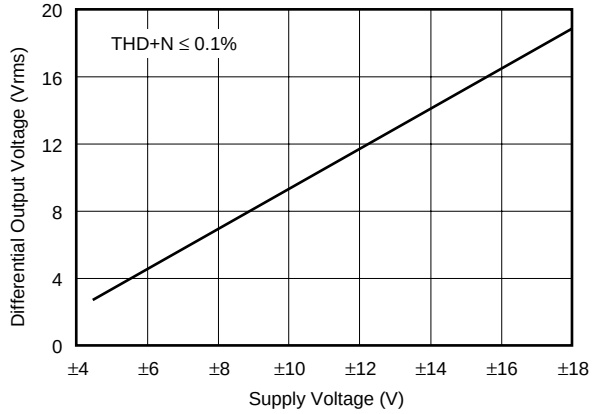
MAXIMUM OUTPUT VOLTAGE SWING vs FREQUENCY



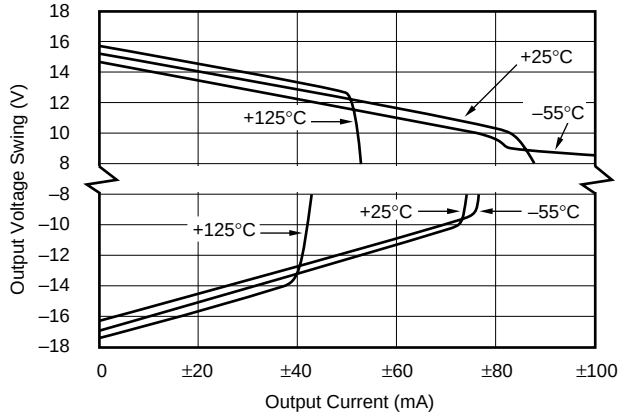
TYPICAL PERFORMANCE CURVES (Cont.)

At T_A = +25°C, V_S = ±18V, R_L = 600Ω differential connected between $+V_O$ and $-V_O$, unless otherwise noted.

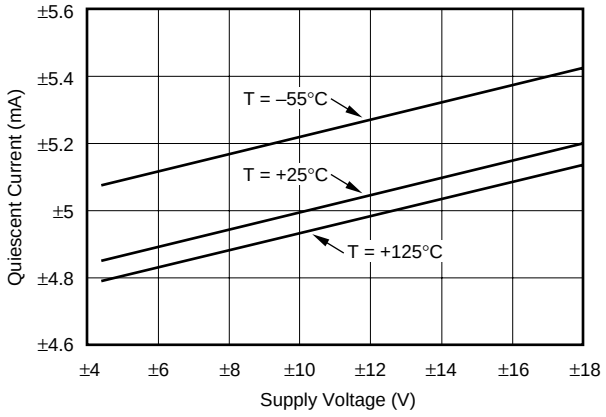
OUTPUT VOLTAGE SWING vs SUPPLY VOLTAGE



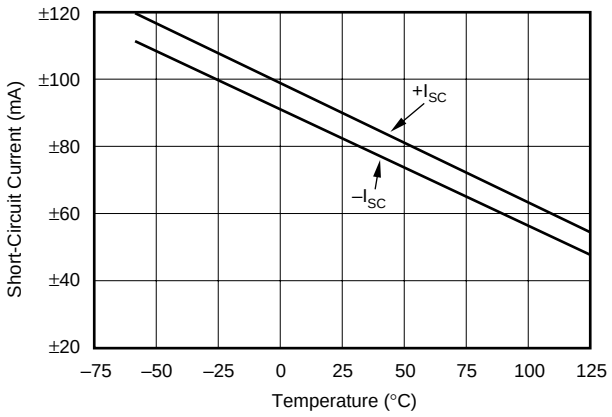
OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



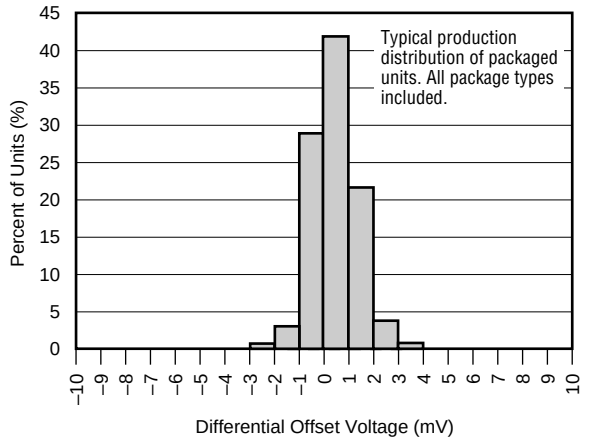
QUIESCENT CURRENT vs SUPPLY VOLTAGE



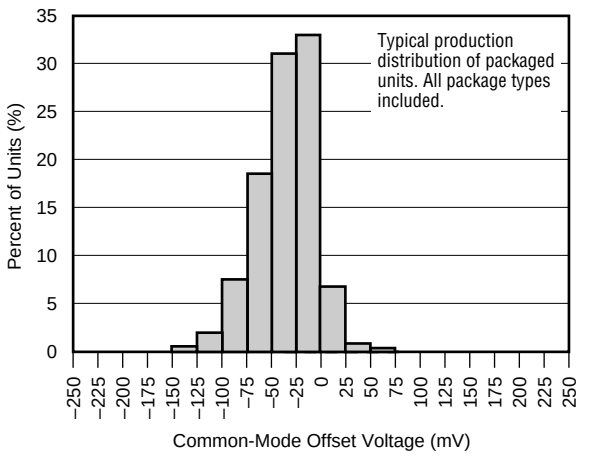
SHORT-CIRCUIT CURRENT vs TEMPERATURE



DIFFERENTIAL OFFSET VOLTAGE PRODUCTION DISTRIBUTION



COMMON-MODE OFFSET VOLTAGE PRODUCTION DISTRIBUTION

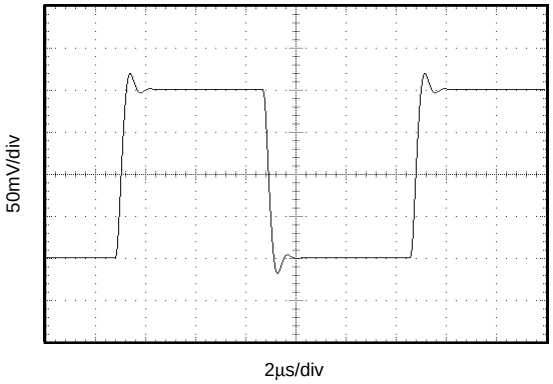


TYPICAL PERFORMANCE CURVES (Cont.)

At T_A = +25°C, V_S = ±18V, R_L = 600Ω differential connected between $+V_O$ and $-V_O$, unless otherwise noted.

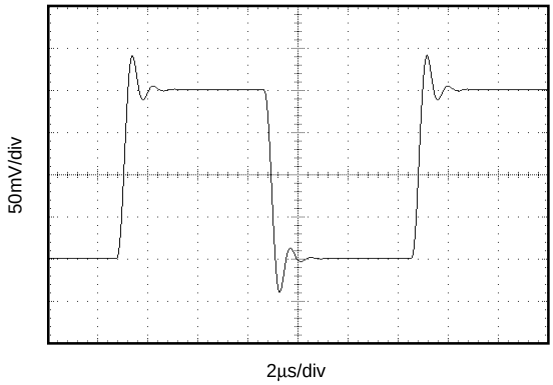
SMALL-SIGNAL STEP RESPONSE

C_L = 100pF



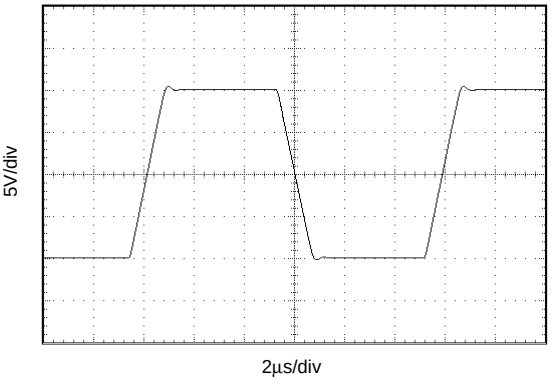
SMALL-SIGNAL STEP RESPONSE

C_L = 1000pF



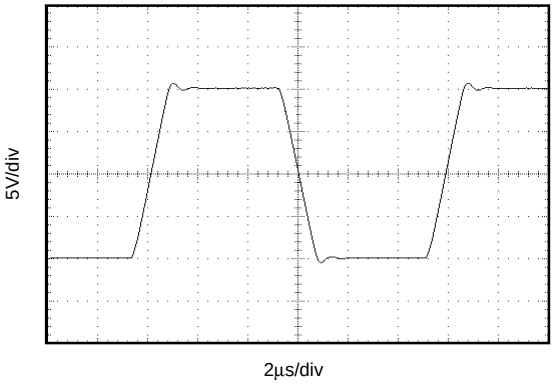
LARGE-SIGNAL STEP RESPONSE

C_L = 100pF

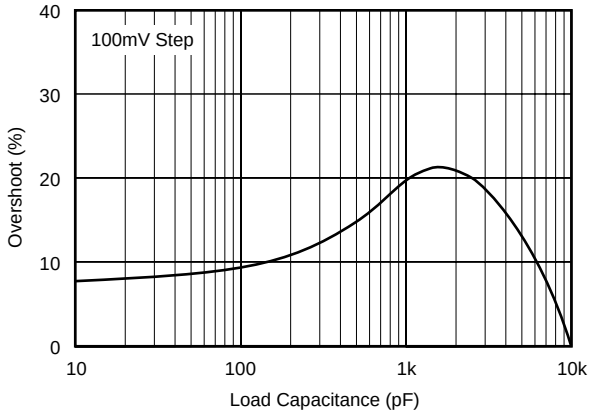


LARGE-SIGNAL STEP RESPONSE

C_L = 1000pF



SMALL-SIGNAL OVERSHOOT
vs LOAD CAPACITANCE



APPLICATIONS INFORMATION

The DRV134 (and DRV135 in SO-8 package) converts a single-ended, ground-referenced input to a floating differential output with +6dB gain (G = 2). Figure 1 shows the basic connections required for operation. Decoupling capacitors placed close to the device pins are strongly recommended in applications with noisy or high impedance power supplies.

The DRV134 consists of an input inverter driving a cross-coupled differential output stage with 50Ω series output resistors. Characterized by low differential-mode output impedance (50Ω) and high common-mode output impedance (1.6kΩ), the DRV134 is ideal for audio applications. Normally, $+V_O$ is connected to +Sense, $-V_O$ is connected to –Sense, and the outputs are taken from these junctions as shown in Figure 1. For applications with large dc cable offset errors, a 10µF electrolytic nonpolarized blocking capacitor at each sense pin is recommended as shown in Figure 2.

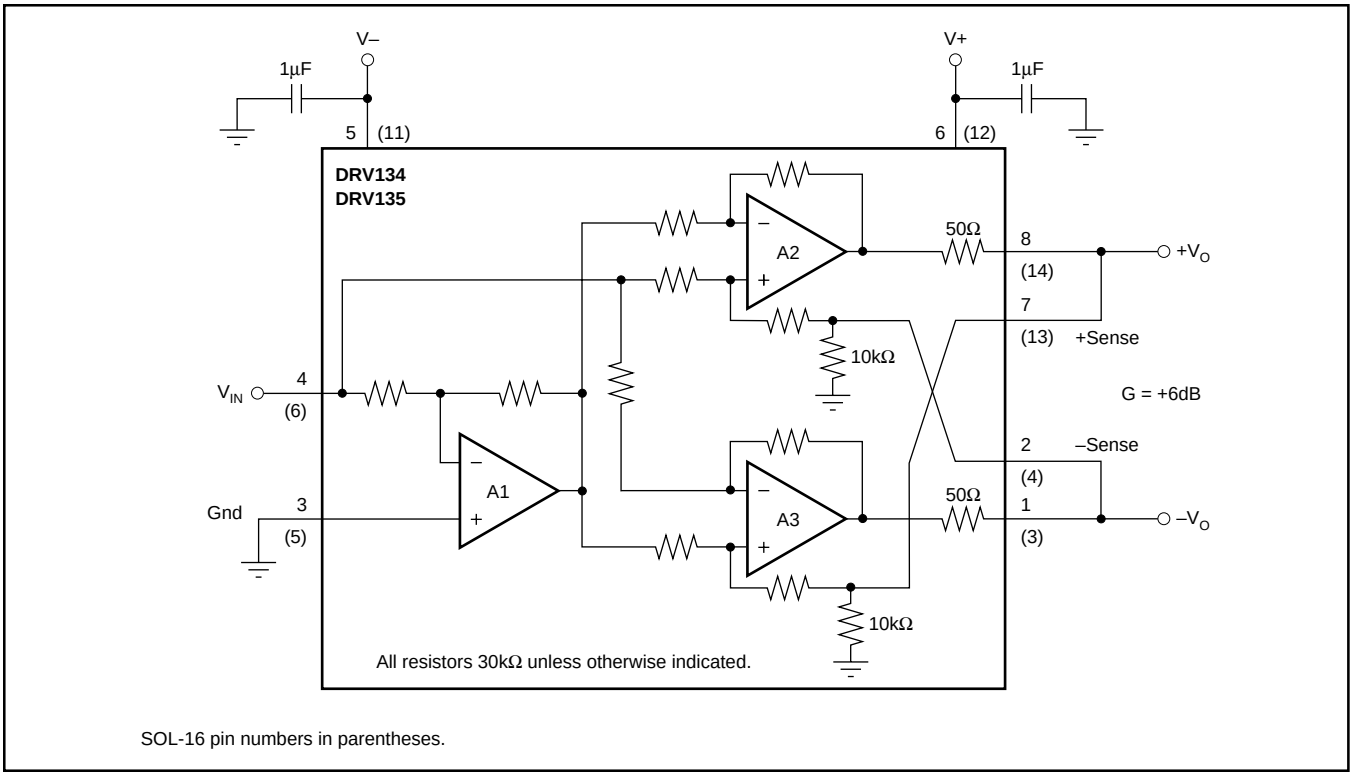


FIGURE 1. Basic Connections.

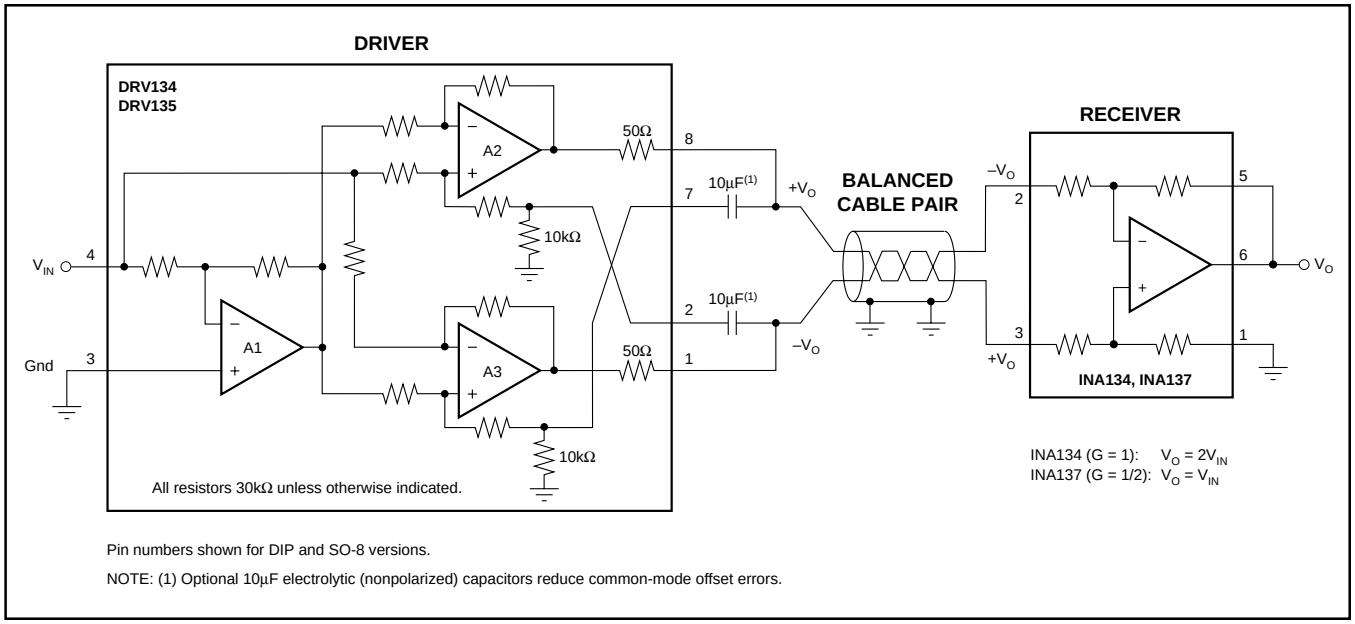


FIGURE 2. Complete Audio Driver/Receiver Circuit.

Excellent internal design and layout techniques provide low signal distortion, high output level (+27dBu), and a low noise floor (–98dBu). Laser trimming of thin film resistors assures excellent output common-mode rejection (OCMR) and signal balance ratio (SBR). In addition, low dc voltage offset reduces errors and minimizes load currents.

For best system performance, it is recommended that a high input-impedance difference amplifier be used as the receiver. Used with the INA134 (G = 0dB) or the INA137 (G = ±6dB) differential line receivers, the DRV134 forms a complete solution for driving and receiving audio signals, replacing input and output coupling transformers commonly used in professional audio systems (Figure 2). When used with the INA137 (G = –6dB) overall system gain is unity.

AUDIO PERFORMANCE

The DRV134 was designed for enhanced ac performance. Very low distortion, low noise, and wide bandwidth provide superior performance in high quality audio applications. Laser-trimmed matched resistors provide optimum output common-mode rejection (typically 68dB), especially when compared to circuits implemented with op amps and discrete precision resistors. In addition, high slew rate (15V/µs) and fast settling time (2.5µs to 0.01%) ensure excellent dynamic response.

The DRV134 has excellent distortion characteristics. As shown in the distortion data provided in the typical performance curves, THD+Noise is below 0.003% throughout the audio frequency range under various output conditions. Both differential and single-ended modes of operation are shown. In addition, the optional 10µF blocking capacitors used to minimize V_{OCM} errors have virtually no effect on performance. Measurements were taken with an Audio Precision System One (with the internal 80kHz noise filter) using the THD test circuit shown in Figure 3.

Up to approximately 10kHz, distortion is below the measurement limit of commonly used test equipment. Furthermore, distortion remains relatively constant over the wide output voltage swing range (approximately 2.5V from the positive supply and 1.5V from the negative supply). A special output stage topology yields a design with minimum distortion variation from lot-to-lot and unit-to-unit. Furthermore, the small and large signal transient response curves demonstrate the DRV134's stability under load.

OUTPUT COMMON-MODE REJECTION

Output common-mode rejection (OCMR) is defined as the change in differential output voltage due to a change in output common-mode voltage. When measuring OCMR, V_{IN} is grounded and a common-mode voltage, V_{CM}, is applied to the output as shown in Figure 4. Ideally no differential mode signal (V_{OD}) should appear. However, a small mode-conversion effect causes an error signal whose magnitude is quantified by OCMR.

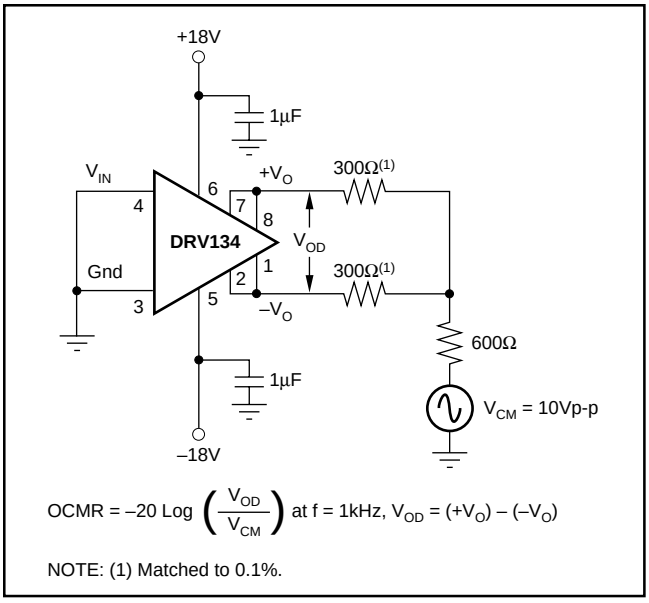


FIGURE 4. Output Common-Mode Rejection Test Circuit.

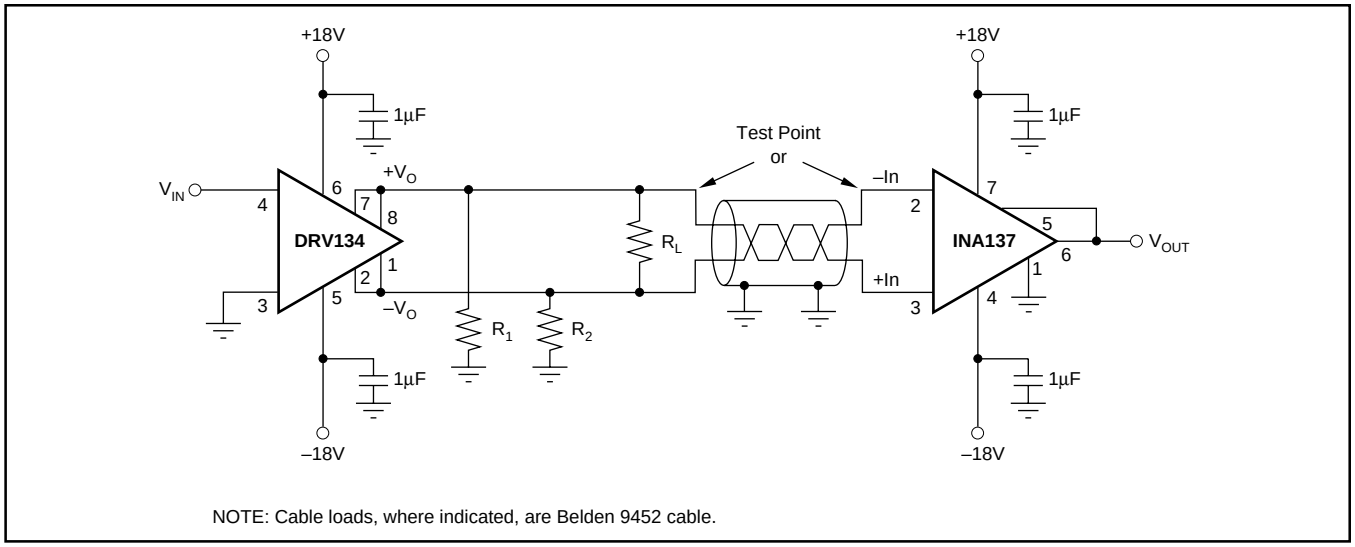


FIGURE 3. Distortion Test Circuit.

SIGNAL BALANCE RATIO

Signal balance ratio (SBR) measures the symmetry of the output signals under loaded conditions. To measure SBR an input signal is applied and the outputs are summed as shown in Figure 5. V_{OUT} should be zero since each output ideally is exactly equal and opposite. However, an error signal results from any imbalance in the outputs. This error is quantified by SBR. The impedances of the DRV134's out put stages are closely matched by laser trimming to minimize SBR errors. In an application, SBR also depends on the balance of the load network.

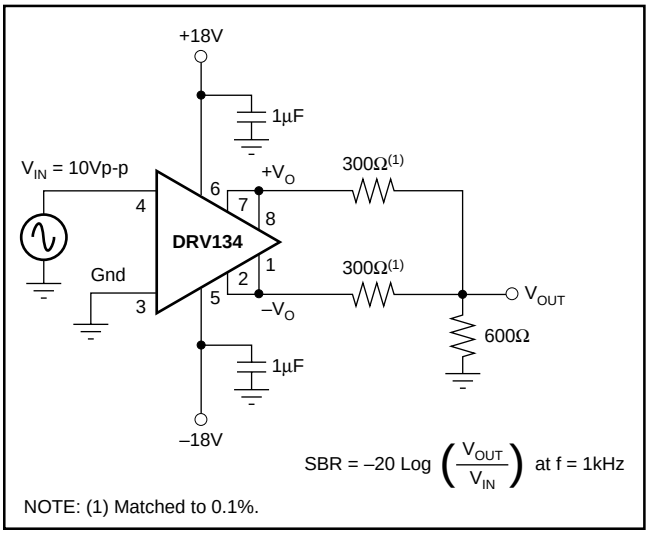


FIGURE 5. Signal Balance Ratio Test Circuit.

SINGLE-ENDED OPERATION

The DRV134 can be operated in single-ended mode without degrading output drive capability. Single-ended operation requires that the unused side of the output pair be grounded (both the V_O and Sense pins) to a low impedance return path. Gain remains +6dB. Grounding the negative outputs as shown in Figure 6 results in a noninverted output signal (G = +2) while grounding the positive outputs gives an inverted output signal (G = –2).

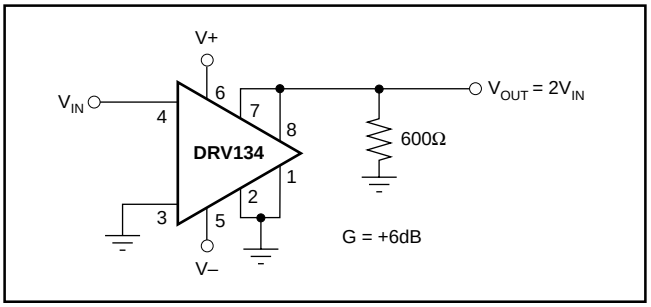


FIGURE 6. Typical Single-Ended Application.

For best rejection of line noise and hum differential mode operation is recommended. However, single-ended performance is adequate for many applications. In general single-ended performance is comparable to differential mode (see THD+N typical performance curves), but the common-mode and noise rejection inherent in balanced-pair systems is lost.

CABLE

The DRV134 is capable of driving large signals into 600Ω loads over long cables. Low impedance shielded audio cables such as the standard Belden 8451 or 9452 (or similar) are recommended, especially in applications where long cable lengths are required.

THERMAL PERFORMANCE

The DRV134 and DRV135 have robust output drive capability and excellent performance over temperature. In most applications there is no significant difference between the DIP, SOL-16, and SO-8 packages. However, for applications with extreme temperature and load conditions, the SOL-16 (DRV134UA) or DIP (DRV134PA) packages are recommended. Under these conditions, such as loads greater than 600Ω or very long cables, performance may be degraded in the SO-8 (DRV135UA) package.

LAYOUT CONSIDERATIONS

A driver/receiver balanced-pair (such as the DRV134 and INA137) rejects the voltage differences between the grounds at each end of the cable, which can be caused by ground currents, supply variations, etc. In addition to proper bypassing, the suggestions below should be followed to achieve optimal OCMR and noise rejection.

- The DRV134 input should be driven by a low impedance source such as an op amp or buffer.
- As is the case for any single-ended system, the source's common should be connected as close as possible to the DRV134's ground. Any ground offset errors in the source will degrade system performance.
- Symmetry on the outputs should be maintained.
- Shielded twisted-pair cable is recommended for all applications. Physical balance in signal wiring should be maintained. Capacitive differences due to varying wire lengths may result in unequal noise pickup between the pair and degrade OCMR. Follow industry practices for proper system grounding of the cables.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV134PA	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		DRV134PA	Samples
DRV134PAG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		DRV134PA	Samples
DRV134UA	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		DRV134UA	Samples
DRV134UA/1K	ACTIVE	SOIC	DW	16	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		DRV134UA	Samples
DRV134UA/1KE4	ACTIVE	SOIC	DW	16	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		DRV134UA	Samples
DRV134UAE4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		DRV134UA	Samples
DRV135UA	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		DRV 135UA	Samples
DRV135UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		DRV 135UA	Samples
DRV135UA/2K5E4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		DRV 135UA	Samples
DRV135UAG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		DRV 135UA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

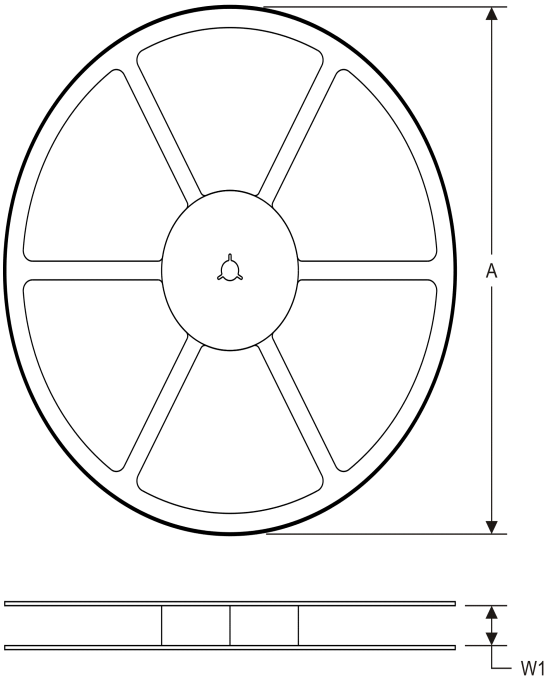
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

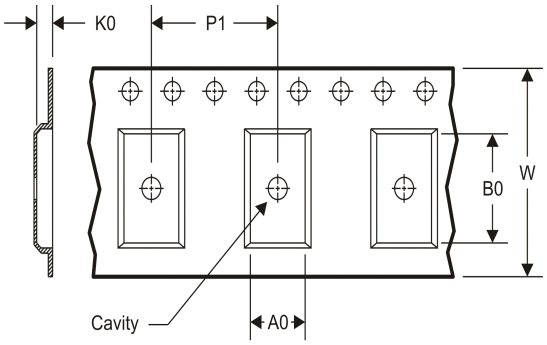
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



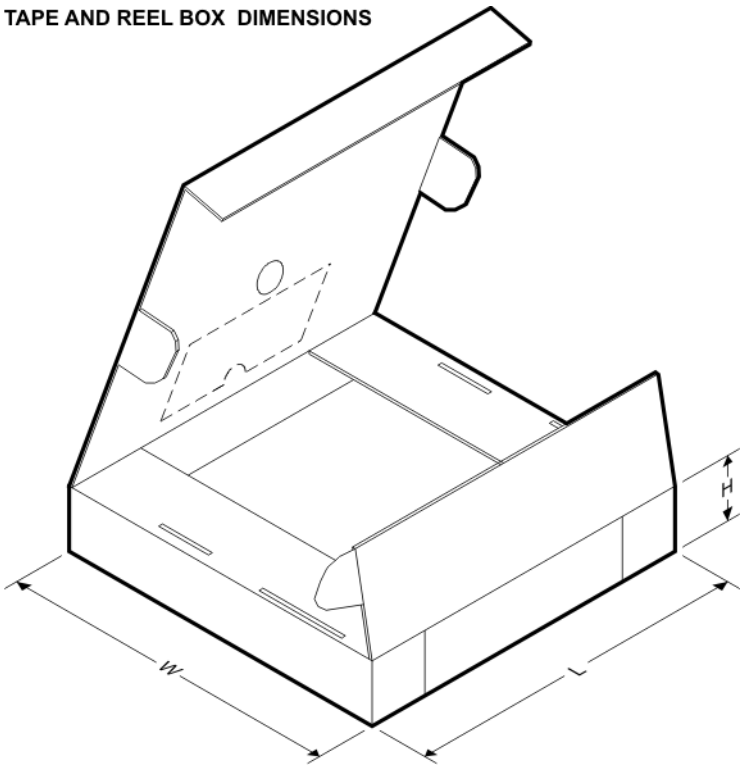
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV134UA/1K	SOIC	DW	16	1000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
DRV135UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

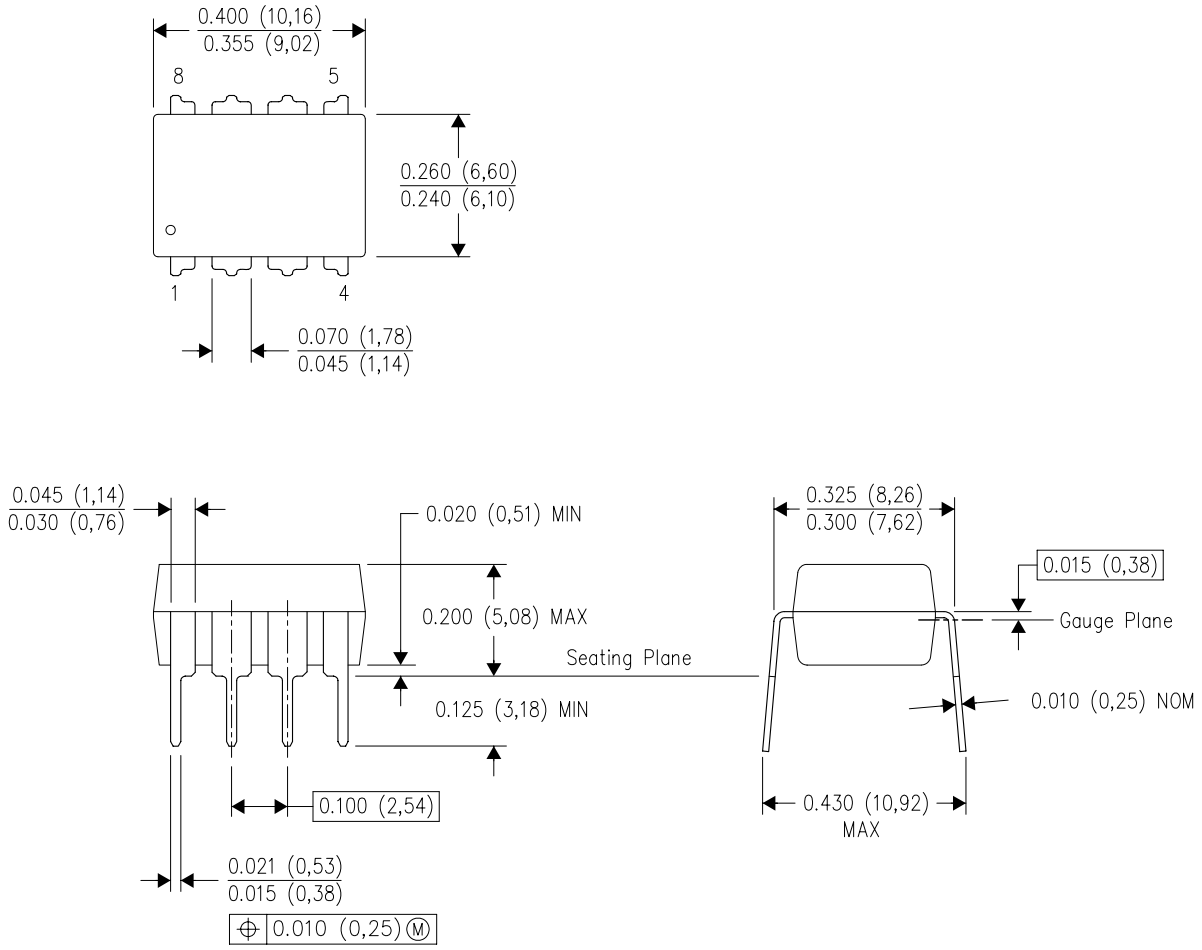
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

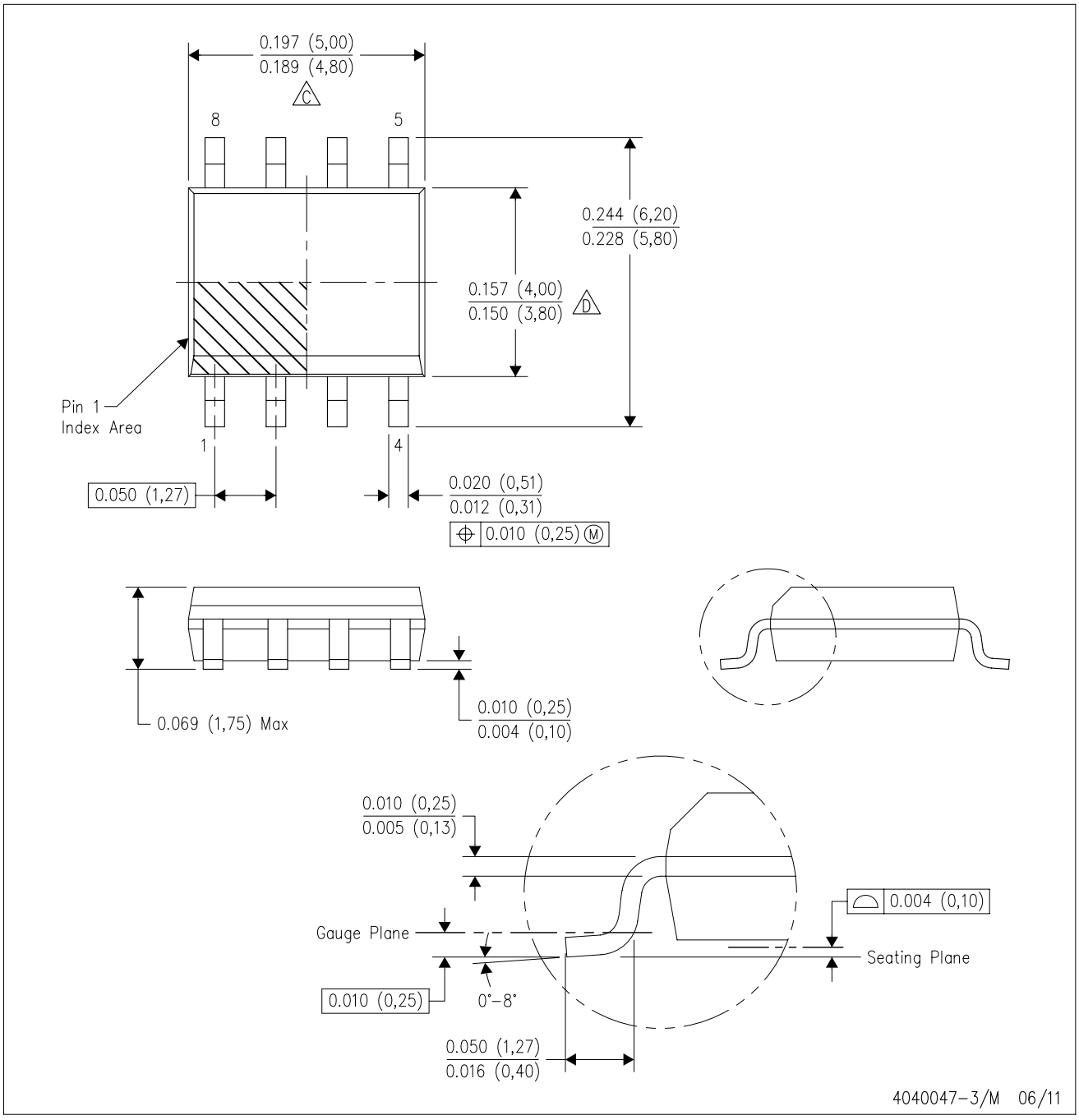
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV134UA/1K	SOIC	DW	16	1000	367.0	367.0	38.0
DRV135UA/2K5	SOIC	D	8	2500	367.0	367.0	35.0

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



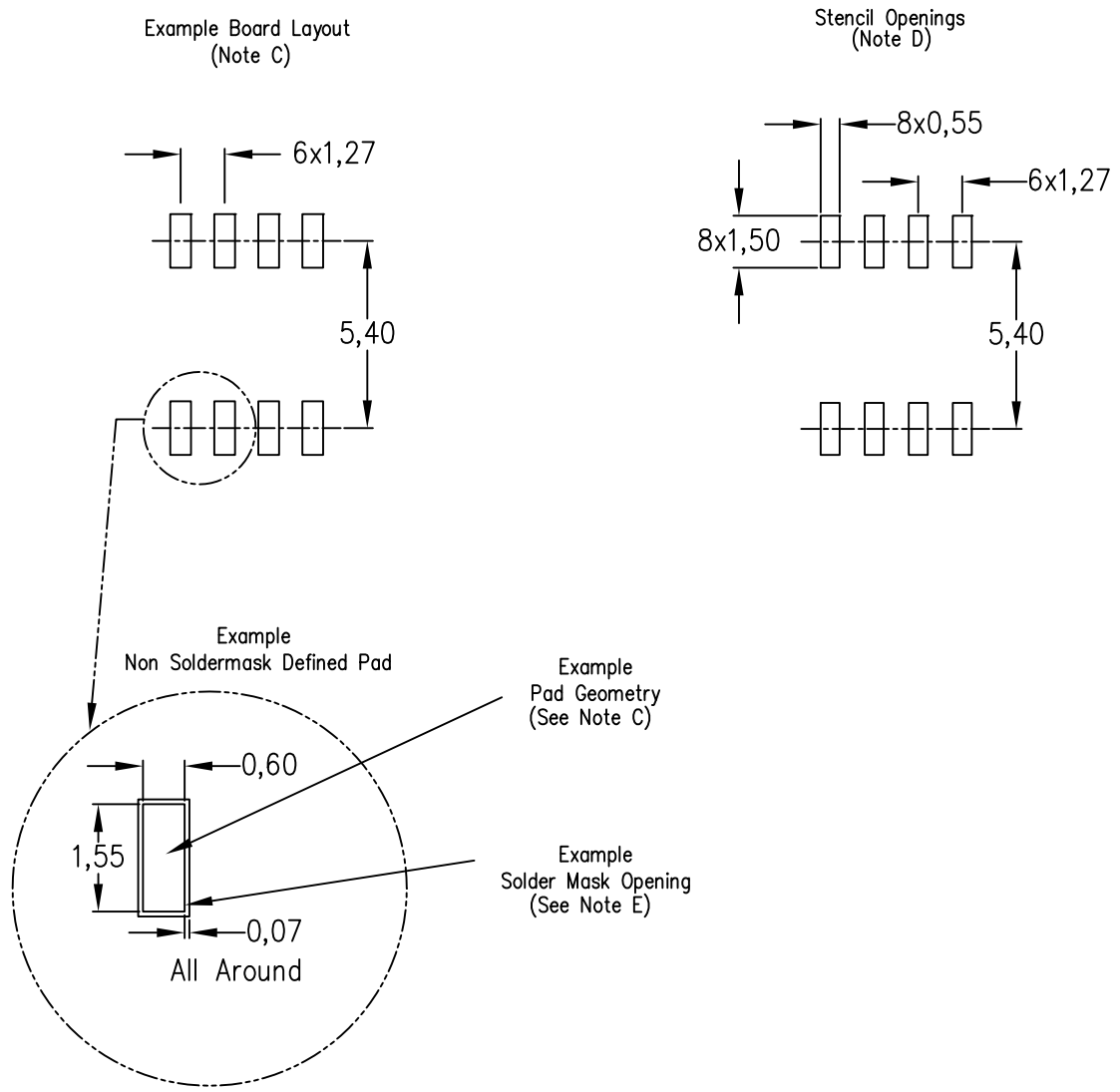
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



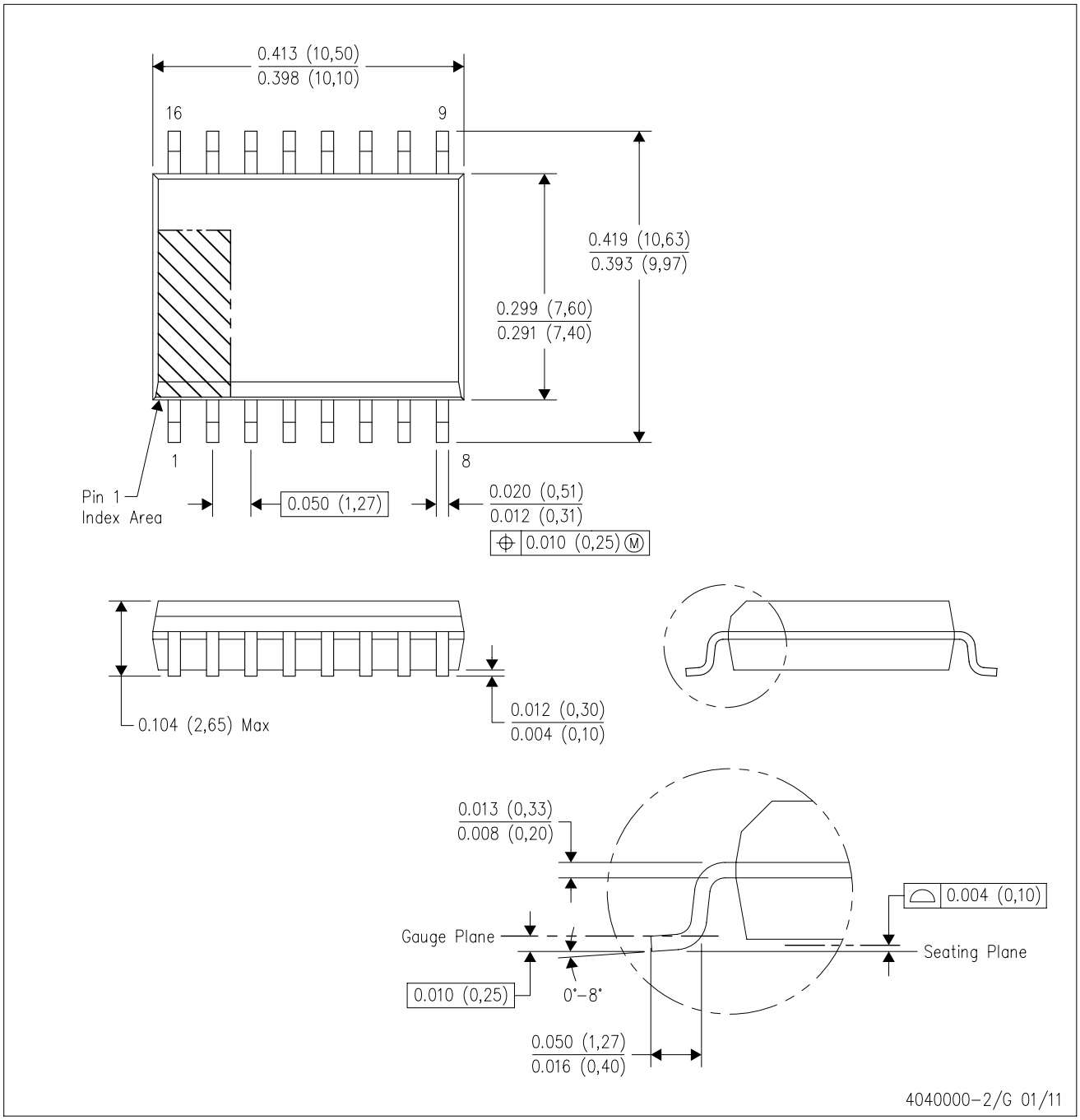
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



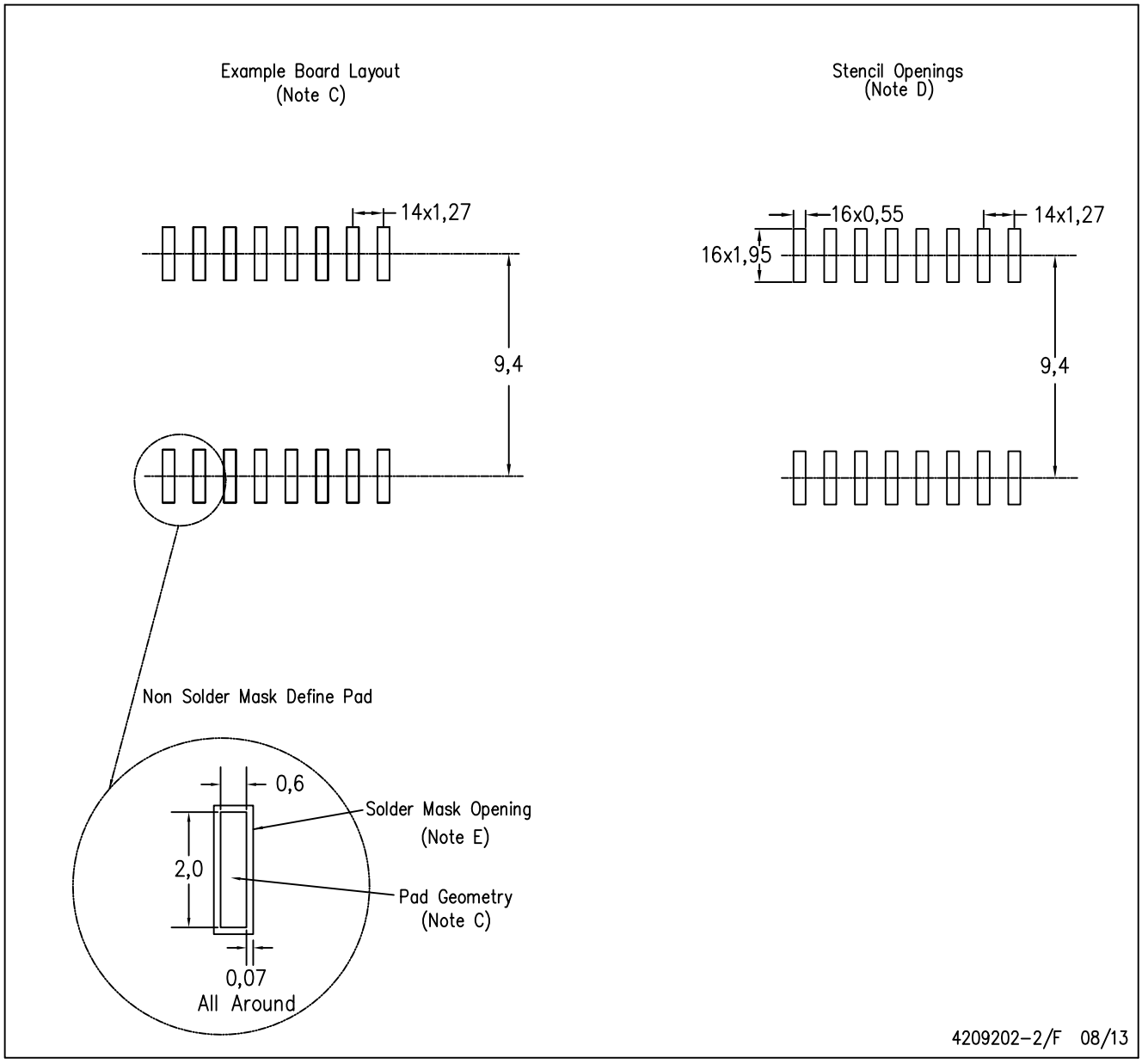
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AA.

DW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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