## DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC


## HEF4076B MSI <br> Quadruple D-type register with 3-state outputs

File under Integrated Circuits, IC04

PHILIPS

## DESCRIPTION

The HEF4076B is a quadruple edge-triggered D-type flip-flop with four data inputs $\left(D_{0}\right.$ to $\left.D_{3}\right)$, two active LOW data enable inputs ( $\overline{E D}_{0}$ and $\left.\overline{E D}_{1}\right)$, a common clock input (CP), four 3-state outputs ( $\mathrm{O}_{0}$ to $\mathrm{O}_{3}$ ), two active LOW output enable inputs ( $\overline{\mathrm{EO}}_{0}$ and $\left.\overline{\mathrm{EO}}_{1}\right)$, and an overriding asynchronous master reset input (MR).


Fig. 1 Functional diagram.

## PINNING

$\mathrm{D}_{0}$ to $\mathrm{D}_{3}$
$\overline{\mathrm{ED}}_{0}, \overline{\mathrm{ED}}_{1}$
$\overline{\mathrm{EO}}_{0}, \overline{\mathrm{EO}}_{1}$
CP
MR
$\mathrm{O}_{0}$ to $\mathrm{O}_{3}$
data inputs
data enable inputs (active LOW)
output enable inputs (active LOW)
clock input (LOW to HIGH, edge-triggered)
master reset input
data outputs

Information on $D_{0}$ to $D_{3}$ is stored in the four flip-flops on the LOW to HIGH transition of CP if both $\overline{E D}_{0}$ and $\overline{E D}_{1}$ are LOW. A HIGH on either $\overline{E D}_{0}$ or $\overline{E D}_{1}$ prevents the flip-flops from changing on the LOW to HIGH transition of CP, independent of the information on $D_{0}$ to $D_{3}$. When both $\overline{\mathrm{EO}}_{0}$ and $\overline{\mathrm{EO}}_{1}$ are LOW, the contents of the four flip-flops are available at $\mathrm{O}_{0}$ to $\mathrm{O}_{3}$. A HIGH on either $\overline{\mathrm{EO}}_{0}$ or $\overline{\mathrm{EO}}_{1}$ forces $\mathrm{O}_{0}$ to $\mathrm{O}_{3}$ into the high impedance OFF-state. A HIGH on MR resets all four flip-flops, independent of all other input conditions.


Fig. 2 Pinning diagram.

HEF4076BP(N): 16-lead DIL; plastic
(SOT38-1)
HEF4076BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
HEF4076BT(D): 16-lead SO; plastic (SOT109-1)
( ): Package Designator North America

FAMILY DATA, IDD LIMITS category MSI
See Family Specifications


Fig. 3 Logic diagram.

## FUNCTION TABLE

|  |  |  |  |  | OUTPUTS |
| :---: | :---: | :---: | :---: | :---: | :---: |
| MR | CP | $\overline{\mathbf{E D}}_{\mathbf{0}}$ | $\overline{\mathbf{E D}}_{\mathbf{1}}$ | $\mathbf{D}_{\mathbf{n}}$ | $\mathbf{o}_{\mathbf{n}}$ |
| H | X | X | X | X | L |
| L | $\nearrow$ | H | X | X | no change |
| L | $\nearrow$ | X | H | X | no change |
| L | $\nearrow$ | L | L | H | H |
| L | $\nearrow$ | L | L | L | L |
| L | L | X | X | X | no change |

## Notes

1. $\overline{\mathrm{EO}}_{0}=\overline{\mathrm{EO}}_{1}=\mathrm{LOW}$

When either $\overline{\mathrm{EO}}_{0}$ or $\overline{\mathrm{EO}}_{1}$ is HIGH , the outputs are disabled (high impedance OFF-state).
$\mathrm{H}=\mathrm{HIGH}$ state (the more positive voltage)
L = LOW state (the less positive voltage)
$\mathrm{X}=$ state is immaterial
$\Gamma=$ positive-going transition
L = negative-going transition

## AC CHARACTERISTICS

$\mathrm{V}_{\mathrm{SS}}=0 \mathrm{~V} ; \mathrm{T}_{\mathrm{amb}}=25^{\circ} \mathrm{C} ; \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$; input transition times $\leq 20 \mathrm{~ns}$; see also waveforms Fig. 4

|  | $\mathrm{V}_{\mathrm{DD}}$ | SYMBOL | MIN. TYP. | MAX. |  | TYPICAL EXTRAPOLATION FORMULA |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Propagation delays $\mathrm{CP} \rightarrow \mathrm{O}_{\mathrm{n}}$ <br> HIGH to LOW <br> LOW to HIGH $\mathrm{MR} \rightarrow \mathrm{O}_{\mathrm{n}}$ <br> HIGH to LOW | $\begin{array}{r} 5 \\ 10 \\ 15 \end{array}$ | $\mathrm{t}_{\text {PHL }}$ | $\begin{array}{r} 150 \\ 60 \\ 45 \end{array}$ | $\begin{array}{r} 305 \\ 120 \\ 85 \end{array}$ | ns <br> ns ns | $\begin{aligned} 123 \mathrm{~ns} & +(0,55 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \\ 49 \mathrm{~ns} & +(0,23 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \\ 37 \mathrm{~ns} & +(0,16 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \end{aligned}$ |
|  | $\begin{array}{r} 5 \\ 10 \\ 15 \end{array}$ | $\mathrm{t}_{\text {PL }}$ | $\begin{array}{r} \hline 160 \\ 65 \\ 45 \end{array}$ | $\begin{array}{r} \hline 320 \\ 130 \\ 90 \end{array}$ | ns ns ns | $\begin{aligned} \hline 133 \mathrm{~ns} & +(0,55 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \\ 54 \mathrm{~ns} & +(0,23 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \\ 37 \mathrm{~ns} & +(0,16 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \end{aligned}$ |
|  | $\begin{array}{r} 5 \\ 10 \\ 15 \end{array}$ | $\mathrm{t}_{\text {PHL }}$ | $\begin{aligned} & 95 \\ & 40 \\ & 30 \end{aligned}$ | $\begin{array}{r} 190 \\ 85 \\ 65 \\ \hline \end{array}$ | ns <br> ns <br> ns | $\begin{aligned} & 68 \mathrm{~ns}+(0,55 \mathrm{~ns} / \mathrm{pF}) C_{\mathrm{L}} \\ & 29 \mathrm{~ns}+(0,23 \mathrm{~ns} / \mathrm{pF}) C_{\mathrm{L}} \\ & 22 \mathrm{~ns}+(0,16 \mathrm{~ns} / \mathrm{pF}) C_{\mathrm{L}} \end{aligned}$ |
| Output transition times HIGH to LOW | $\begin{array}{r} 5 \\ 10 \\ 15 \end{array}$ | ${ }_{\text {t }}^{\text {H }}$ L | $\begin{aligned} & 60 \\ & 30 \\ & 20 \\ & \hline \end{aligned}$ | $\begin{array}{r} 120 \\ 60 \\ 40 \\ \hline \end{array}$ | ns <br> ns <br> ns | $\begin{aligned} 10 \mathrm{~ns} & +(1,0 \mathrm{~ns} / \mathrm{pF}) C_{\mathrm{L}} \\ 9 \mathrm{~ns} & +(0,42 \mathrm{~ns} / \mathrm{pF}) C_{\mathrm{L}} \\ 6 \mathrm{~ns} & +(0,28 \mathrm{~ns} / \mathrm{pF}) C_{\mathrm{L}} \end{aligned}$ |
| LOW to HIGH | $\begin{array}{r} 5 \\ 10 \\ 15 \end{array}$ | ${ }_{\text {t }}^{\text {L }}$ LH | $\begin{aligned} & \hline 60 \\ & 30 \\ & 20 \\ & \hline \end{aligned}$ | $\begin{array}{r} \hline 120 \\ 60 \\ 40 \\ \hline \end{array}$ | ns <br> ns <br> ns | $\begin{aligned} & \hline 10 \mathrm{~ns}+(1,0 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \\ & 9 \mathrm{~ns}+(0,42 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \\ & 6 \mathrm{~ns}+(0,28 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \\ & \hline \end{aligned}$ |
| 3-state propagation times Output disable times $\overline{\mathrm{EO}}_{n} \rightarrow \mathrm{O}_{\mathrm{n}}$ <br> HIGH <br> LOW | $\begin{array}{r} 5 \\ 10 \\ 15 \end{array}$ | $t_{\text {PHZ }}$ | $\begin{aligned} & 50 \\ & 35 \\ & 30 \end{aligned}$ | $\begin{array}{r} 105 \\ 70 \\ 65 \end{array}$ | ns <br> ns <br> ns |  |
|  | $\begin{array}{r} 5 \\ 10 \\ 15 \end{array}$ | tpLZ | $\begin{aligned} & 45 \\ & 30 \\ & 30 \end{aligned}$ | 90 65 60 | ns <br> ns <br> ns |  |


|  | $\mathrm{V}_{\mathrm{DD}}$ | SYMBOL | MIN. TYP. | MAX. |  | TYPICAL EXTRAPOLATION FORMULA |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Output enable times $\overline{\mathrm{EO}}_{\mathrm{n}} \rightarrow \mathrm{O}_{\mathrm{n}}$ <br> HIGH | 5 | $t_{\text {PzH }}$ | 65 | 130 | ns |  |
|  | 10 |  | 30 | 55 | ns |  |
|  | 15 |  | 20 | 40 | ns |  |
|  | 5 |  | 60 | 120 | ns |  |
| LOW | 10 | $\mathrm{t}_{\text {PZL }}$ | 25 | 50 | ns |  |
|  | 15 |  | 20 | 35 | ns |  |

## AC CHARACTERISTICS

$\mathrm{V}_{\mathrm{SS}}=0 \mathrm{~V} ; \mathrm{T}_{\mathrm{amb}}=25^{\circ} \mathrm{C} ; \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$; input transition times $\leq 20 \mathrm{~ns}$
$\left.\begin{array}{|c|r|l|rrr|r|}\hline & \mathbf{V}_{\text {DD }} & \text { SYMBOL } & \text { MIN. } & \text { TYP. } & \text { MAX. } & \text { TYPICAL EXTRAPOLATION } \\ \text { FORMULA }\end{array}\right]$

|  | $V_{D D}$ <br> $\mathbf{V}$ | TYPICAL FORMULA FOR $\mathbf{P}(\mu \mathrm{W})$ |  |
| :--- | :---: | :---: | :--- |
| Dynamic power | 5 | $2200 \mathrm{f}_{\mathrm{i}}+\sum\left(\mathrm{f}_{0} \mathrm{C}_{\mathrm{L}}\right) \times \mathrm{V}_{\mathrm{DD}}{ }^{2}$ | where |
| dissipation per | 10 | $9300 \mathrm{f}_{\mathrm{i}}+\sum\left(\mathrm{f}_{0} \mathrm{C}_{\mathrm{L}}\right) \times \mathrm{V}_{\mathrm{DD}}{ }^{2}$ | $\mathrm{f}_{\mathrm{i}}=$ input freq. $(\mathrm{MHz})$ |
| package (P) | 15 | $24500 \mathrm{f}_{\mathrm{i}}+\sum\left(\mathrm{f}_{0} \mathrm{C}_{\mathrm{L}}\right) \times \mathrm{V}_{\mathrm{DD}}{ }^{2}$ | $\mathrm{f}_{\mathrm{o}}=$ output freq. $(\mathrm{MHz})$ |
|  |  | $\mathrm{C}_{\mathrm{L}}=$ load capacitance $(\mathrm{pF})$ |  |
|  |  | $\sum\left(\mathrm{f}_{0} C_{L}\right)=$ sum of outputs |  |
|  |  | $\mathrm{V}_{\mathrm{DD}}=$ supply voltage $(\mathrm{V})$ |  |


Fig. 4 Waveforms showing propagation delays, output disable/enable times, minimum CP and MR pulse widths, set-up and hold times for $D_{n}$ to $C P$ and $\overline{E D}_{n}$ to $C P$, and recovery time for MR. Set-up and hold times are shown as positive values but may be specified as negative values.

